

Measurement and Characterization of FET Devices Using EKV Parameters Applied to POSFET Sensors

Arun Kumar Sinha

Abstract—This paper presents an algorithm to extract the EKV parameters using the input characteristic measurement. The working of the algorithm was verified by extracting a parameter through the pinch-off characteristic measurement. The extraction and measurement was performed on FET devices present in Piezo-Electric Oxide Semiconductor Field Effect Transistor (POSFET) sensor. Using the extracted parameters we fixed the region of operation of this sensor at weak inversion.

Index Terms—Algorithms, flowcharts, piezoelectric semiconductor, semiconductor device measurements.

I. INTRODUCTION

Measurement and characterization of electrical sensor is very important for optimal dynamic response of the sensor. The importance is more when sensor is based on transistor array. The tactile sensors called by the name Piezo-electric Oxide Semiconductor Field Effect Transistor (POSFET) as reported in [1]; have the PolyVinylidene Fluoride (PVDF) on the floating gate of the NMOS transistor arrays. The biasing of such sensor is very important to better utilize the dynamic response by the piezo-electric polymer. Therefore only important parameters need to be extracted for biasing the transistor of the sensor. One method of biasing these sensors has been reported in [2]. The graphical based method was quick but has limitations due to the following three reasons. First, no any standard method was adopted for extracting the parameters from the transistor on a sensor chip. Second, the region of inversion was not fixed before biasing the sensors. Third, in absence of PVDF model of the POSFET sensor, it is very critical to assume the small signal model. Because the dynamic voltage generated by the polymer can be comparable to the gate overdrive voltage. In such case it was worth to consider the large signal model of the transistor.

In this paper we will present the extraction and measurement of the EKV parameters [3] using our proposed algorithm. The choice of EKV equation is due to the fact that it is applicable to all the regions of inversion. Our algorithm uses input characteristic measurement to determine the EKV parameters in a single run. To verify the algorithm we will extract one parameter through pinch-off characteristic

measurement [4]. Using the extracted parameters and large signal equation we will fix the bias point of POSFET sensor for maximum gain. The top metal layer of the POSFET was connected to the supply voltage.

The layout of this paper is as follow: Section II will give an architectural overview of the sensor. In section III we will present the EKV equation and the important parameters for characterizing the sensor. In section IV we will present the algorithm based on Matlab[®] for extracting the parameters. In section V using the extracted parameters, we will size the common drain resistance. In section VI we will present the results of our extraction and measurement. Finally, in section VII we made conclusion of this paper.

II. DESCRIPTION OF POSFETS

The POSFET chip is organized in 5 rows and 5 columns as shown in Fig. 1 (25 in total) [1]. The NFET is a part of the POSFET chip and was obtained by using a non-standard ion-sensitive field effect transistor ISFET/NMOS; p-well technology fabrication process derived from a 4 μm Al-gate with a SiO₂/Si₃N₄ double layer gate dielectric. The MOS gates are designed by using an “inter-digitized” structure with channel width $W = 7500 \mu\text{m}$ and length $L = 12 \mu\text{m}$.

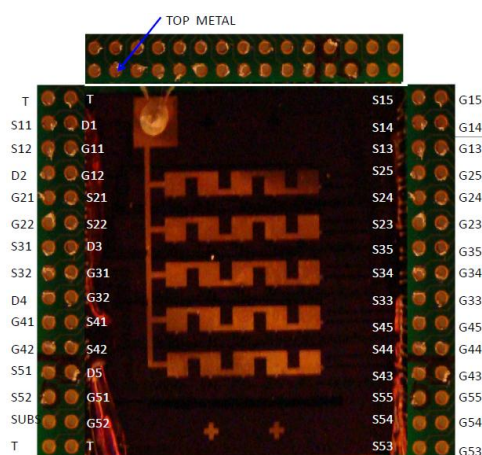


Fig. 1. Chip package photo and its pin-out (S = Source, D = Drain, G = Gate, SUBS = Substrate and T = Temperature sensing diodes).

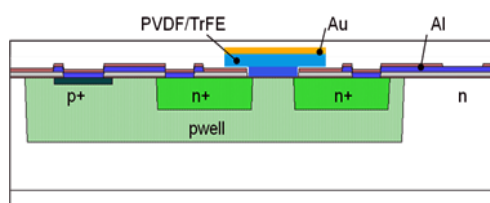


Fig. 2. FET cross section in POSFET sensor.

The NFET was realized starting from n-type, 4 inches

Manuscript received December 30, 2012; revised July 23, 2013. This work is supported by the European Commission project "ROBOSKIN", under grant agreement no. 231500.

Arun Kumar Sinha is with the Department of Electrical, Electronic and Telecommunication Engineering, and Naval Architecture, University of Genoa, Genoa, Italy (e-mail: arun.kumar.sinha@unige.it).

silicon wafers by using implanted n+ source and drain regions on p-well in order to insulate the devices from the n-type substrate (see Fig. 2). The p-well has a junction depth of 4.76 μm and sheet resistance of 3.5 k Ω /sq. The PVDF-TrFE a co-polymer of PVDF was spin coated with thickness 2.5 μm on the gate. The top contact is implemented with an evaporated gold electrode. Poling of the piezoelectric polymer is performed at chip level using the gold top metal and Al contacts of the gate. The POSFETs are working in common drain configuration with floating gate. All the top metals and the drain of the NFETs in a row were separately connected together.

III. EKV EQUATION AND THE ESSENTIAL PARAMETERS

The EKV equations are based on the charge sheet model dedicated for low power and low voltage design. In order to maintain the device symmetry, the terminals were referenced w.r.t. well/substrate. In fact the equations were first derived for weak and strong inversion, then normalized and linked using interpolation function [3]. Therefore we have an equation valid for all the regions of inversion. The EKV equation is given by,

$$I_{DS} = I_S \left(\ln^2 \left(1 + \exp \left(\frac{V_p - V_S}{2U_T} \right) \right) - \ln^2 \left(1 + \exp \left(\frac{V_p - V_D}{2U_T} \right) \right) \right) \quad (1)$$

In (1), I_S is the specific current, V_p is the pinch-off voltage and U_T is the thermodynamic voltage ($\cong 26 \text{ mV}$ at 27°C). Eq. (1) can be approximated for the weak and strong inversion saturation regions [5]. According to [4], the EKV equation requires following parameters as shown in Table I.

TABLE I: LIST OF EKV PARAMETERS FOR FET

Name	Parameter
Pinch-off voltage	$V_p \cong (V_G - V_{TO})/n(V_G)$
Slope factor	$n = 1 + (\text{GAMMA}/\sqrt{V_p + \text{PHI}})$
Specific current	$I_S = 2 \times n \times K_n(W/L_{\text{eff}}) \times U_T^2$

In Table I, K_n is the normalized transconductance parameter, V_{TO} is the threshold voltage and n is the slope factor which depends on the gate voltage (i.e., V_G).

IV. ALGORITHMS FOR EXTRACTION AND MEASUREMENT OF THE EKV PARAMETERS

In this section we will present the algorithms for extracting and measuring the EKV parameters of a NMOS transistor (i.e., wide width and long channel). For extraction we will use the input characteristics (i.e., $\log_e(I_{DS})$ versus V_{GS}) measurement reported in [6]. We will separately verify the extraction by measuring the threshold voltage, from pinch-off characteristic of the NFET using Keithley[®] instruments. During measurement the instruments were working in source voltage and measure current mode. The instruments were interfaced to the PC through the Agilent[®] general purpose interface bus (GPIB) and data were acquired using Instrument Control Toolbox[™] (ICT) on Matlab[®]. The program for I-V measurement was written on M-files using

Device Dependent Commands (DDC) and Standard Commands for Programm-able Instrument (SCPI) language of Keithley[®] 236 and Keithley[®] 2400 instruments. Fig. 3 shows the flowchart comparing our method with the EKV method of parameters extraction. Thus our extraction method can determine very quickly all the three parameters namely; V_{TO} , I_S and n_n of EKV equation in one run.

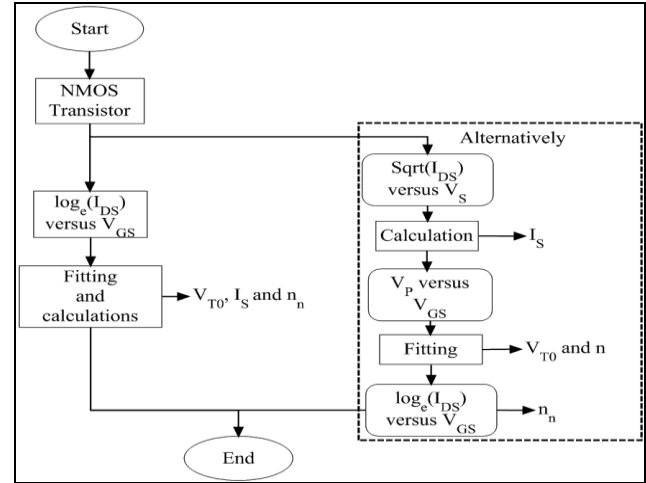


Fig. 3. Proposed flowchart for extracting EKV parameters.

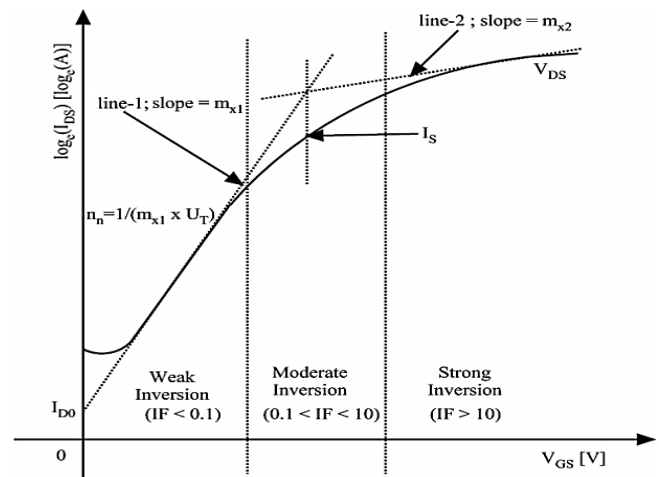


Fig. 4. Different inversion regions depicted by input characteristic curve.

Fig. 4 shows different regions of inversion depicted by the input characteristic curve [7]. The ratio of I_{DSsat} and I_S is called as inversion factor (IF), at middle of moderate inversion $IF = 1$ and this can determine the value of I_S . When straight line is extrapolated from weak and from strong inversion region; the intersection of the two lines can approximately determine the value of specific current. For estimating the V_{TO} , first we will determine the slope factor at weak inversion (n_n) and I_{D0} (residual drain current in saturation for $V_G = V_S = 0$). The slope factor at weak inversion as shown in Fig. 4 is the inverse of slope of line-1 multiplied with U_T [5]. If I_{D0} is the intersection of the line-1 with the Y-axis, then V_{TO} can be determined as,

$$V_{TO} = -n_n U_T \ln(I_{D0}/I_S). \quad (2)$$

The extraction of all the three EKV parameters were implemented in an automated way on Matlab[®] using the flowchart of Fig. 5. After saving the input characteristics measurements as data points, the data were procured by the

program written on M-File. In this way the three main parameters i.e. threshold voltage, specific current and slope factor at weak inversion, were quickly estimated in one run instead of separate measurements for each parameters.

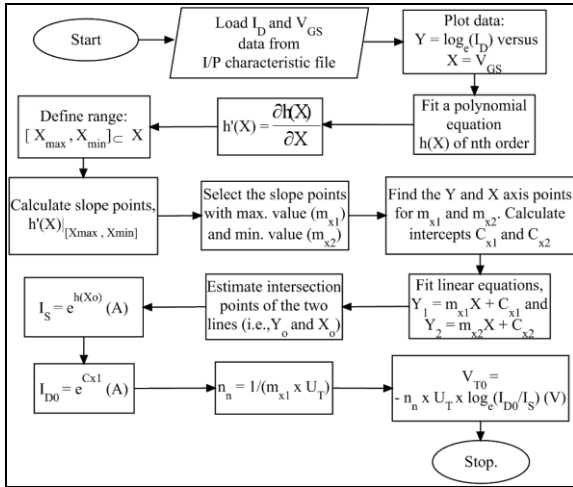


Fig. 5. Flowchart of the algorithm to extract the EKV parameters from input characteristic measurement.

To verify the working of our extraction method, we made direct measurement of pinch-off characteristic using Keithley® instruments to estimate the value of V_{TO} . Fig. 6 shows the electrical connection of the POSFET sensor during pinch-off characteristic measurement.

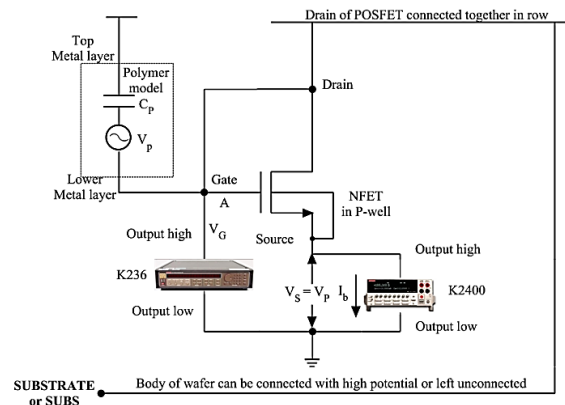


Fig. 6. Electrical connection of POSFET while measuring pinch-off characteristic ("K" mean Keithley®).

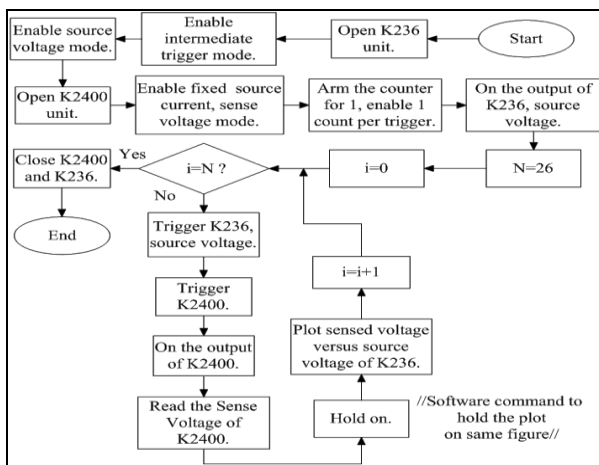


Fig. 7. Flowchart for FET pinch-off measurement ("K" mean Keithley®).

As shown in Fig. 6 the Keithley® 236 source set of gate

voltage V_G to the terminal of diode connected NFET device. The Keithley® 2400 source the constant bias current $I_b (= I_S/2)$ across its terminals and measure the set of source voltage V_S for corresponding sweep of V_G . Finally a figure is plotted between $V_S (= V_P)$ and V_G called as pinch-off characteristic of the NMOS transistor. The algorithm implementing this kind of measurement is shown in Fig. 7.

Fig. 6 shows well to source connected NMOS in POSFET sensor, therefore during measurement the body effect is avoidable and the slope factor is a constant value. If the well was at ground potential then the slope factor will depend on the gate voltage [8]. Thus in our case V_{TO} remain constant and the slope factor is applicable to all regions of inversion. So we can verify our algorithm using the value of V_{TO} obtained from the pinch-off characteristic measurement.

V. DETERMINING THE WORKING REGION OF POSFET

In this section we will present the sizing of the common drain resistance to bias the POSFET sensor by using the extracted parameters. The equations were derived under the condition that the gate was coupled to the supply voltage by a factor A_C which is defined latter in this section. In order to achieve the maximum value of gain by common drain resistance, we will explore the option of weak/moderate inversion for biasing the sensor. Considering the forward current in EKV equation; Eq. (1) can be expressed by,

$$I_{DS} = I_S \times \ln^2 \left(1 + \exp \left(\frac{(V_P - V_S)}{2U_T} \right) \right). \quad (3)$$

For the well to source connected device in saturation $V_{DS} > 4U_T (\cong 0.1 V)$, (3) will reduce to,

$$I_{DSsat} = I_S \times \ln^2 \left(1 + \exp \left(\frac{(V_{GS} - V_{TO})}{2nU_T} \right) \right). \quad (4)$$

Expressing (4) in term of inversion factor, the source voltage (V_S) can be written as,

$$V_S = A_C V_{DD} - \left(V_{TO} + 2nU_T \ln \left(\exp(\sqrt{IF}) - 1 \right) \right). \quad (5)$$

In (5), if C_{PVDF} is the capacitance of the piezo-electric polymer and C_{gate} is the gate capacitance, then the coupling factor is defined as $A_C = C_{PVDF} / (C_{PVDF} + C_{gate})$ and relates the gate voltage of transistor to the supply voltage. The large signal gain A_V will be maximum when $IF < 0.1$ and when $0.1 < IF < 10$ the value of gain will be smaller than maximum [8]. In (5) after substituting the value of V_{TO} , IF , n and A_C ; we will get a value of resistance which can guarantee maximum gain from common drain configuration of transistor as given by,

$$R = V_S / (IF \times I_S). \quad (6)$$

The maximum dynamic from the PVDF on the gate of POSFET sensor is $0.5 V (p)$. The value of resistance should be selected in such a way so that the dynamic signal should not approach the supply rail otherwise it can get distorted.

VI. RESULTS AND DISCUSSION

In this section we will briefly elaborate the results of our algorithm for extraction and the pinch-off characteristics

measurement. Rather than presenting the results for all the FETs, we will present the results of one FET “P15” on the POSFET chip. We will explore the choice of inversion region by considering the value of resistance and source potential. The estimated values of parameters are: $I_S = 0.7314$ mA, $V_{T0} = 2.3$ V and $n = 16.1$; the value of $A_C = 0.782$. The output window after running the extraction program on Matlab[®] is shown in Fig. 8.

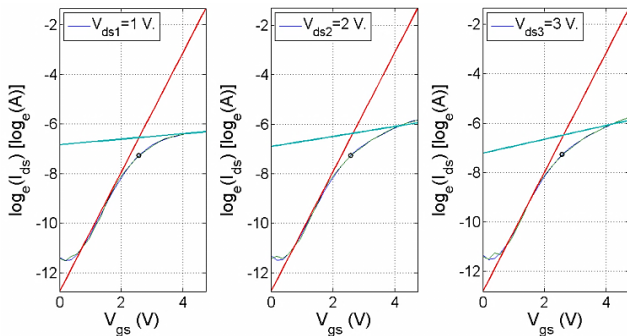


Fig. 8. Extraction results of program output for P15, small bubble indicates the specific current, numerical values of parameters were displayed on the command window.

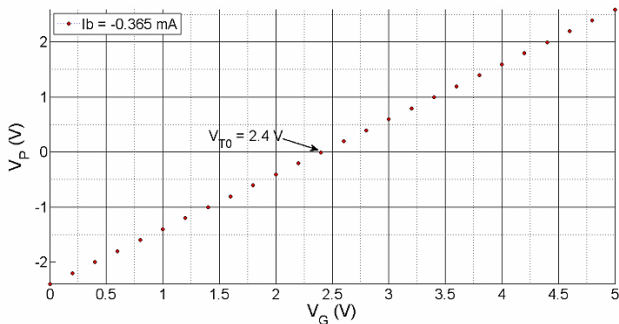


Fig. 9. Measured pinch-off characteristic for P15.

Fig. 9 shows the pinch-off characteristics measurement of the same FET device. The value of V_{T0} shown in Fig. 9 after measurement is 2.4 V which closely coincides with the value given by our algorithm.

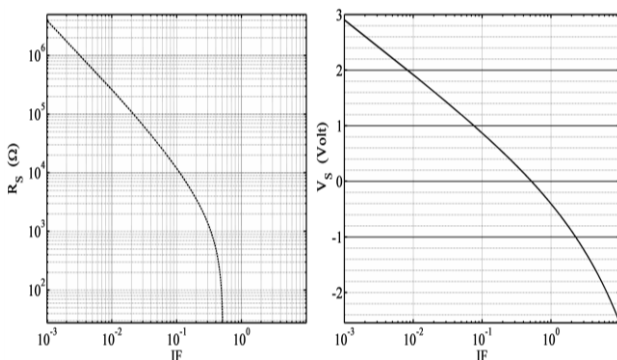


Fig. 10. Variation of resistance and source potential w.r.t. inversion factor.

When the top metal layer of POSFET was fixed to $V_{DD} = 3$ V, the variation of resistance and source voltage w.r.t. the inversion factor for the POSFET is shown in Fig. 10. From

the figure it can be interpreted that, the POSFET can be biased in weak inversion with a suitable value of resistance without approaching supply voltage, in order to have maximum value of dynamic gain by the sensor.

VII. CONCLUSION

We proposed in this paper an algorithm to extract EKV parameters: threshold voltage, specific current and slope factor using the input characteristic measurement. The proposed extraction method was further verified through the direct measurement of the pinch-off characteristic. Using these parameters we explored the region of POSFET operation. We used large signal model of FET, while sizing the value of resistance; and we found that the POSFET can be easily biased in weak inversion for maximum gain.

REFERENCES

- [1] R. S. Dahiya, G. Metta, M. Valle, A. Adami and L. Lorenzelli, “Piezoelectric oxide semiconductor field effect transistor touch sensing devices,” *Appl. Phys. Lett.*, vol. 95, pp. 034 105-1-034 105-3, July 2009.
- [2] L. Barboni, M. Valle, and R. Dahiya, “POSFET touch sensing devices: bias circuit design based on the gm/Id parameter,” in *Proc. 16th Annual Conf. on Sensors and Microsystems*, Rome, Italy, 2011, pp. 1-2.
- [3] C. C. Enz, F. Krummenacher, and E. A. Vittoz, “An analytical MOS transistor valid in all region of operation and dedicated to low-voltage application,” *J. Analog Integr. Circuits and Signal Process.*, vol. 8, pp. 83-114, July 1995.
- [4] M. Bucher, C. Lallement, C. Enz, and F. Krummenacher, “Accurate MOS modeling for analog circuit simulation using the EKV model,” in *Proc. 1996 IEEE Int. Symp. on Circuits and Systems*, Atlanta, GA, USA, vol. 4, pp. 703-706.
- [5] A. Tajalli and Y. Leblebici, *Extreme Low-Power Mixed Signal IC Design*, Springer publications, 2010, ch. 2.
- [6] A. K. Sinha and M. Valle, “A scheme for measuring and extracting level-1 parameters of FET devices applied toward POSFET sensors array,” in *Proc. 23rd Int. Conf. on Microelectronics*, Yasmine Hammamet, Tunisia, 2011, pp. 1-5.
- [7] Y. Tsividis, *Operation and Modeling of the MOS transistor*, New York: Oxford University Press, 1999, ch. 10, pp. 513-543.
- [8] D. Stefanovic and M. Kayal, *Structured Analog CMOS Design*, Springer Publishing Company, 2008, pp. 7-75.



Arun Kumar Sinha was born in Jamshedpur (Jka), India on October 13, 1981. He received the B.Tech degree in electronics and telecommunication engineering from N.I.T. Kurukshetra (Deemed University), India, in 2004 and the M.Tech (honours) degree in process control engineering from the Netaji Subhas Institute of Technology (affiliated to Delhi University), India, in 2007.

In 2007, he joined Agilent Technologies in Gurgaon, India, as a R&D Engineer. Then in 2008, he joined Netaji Subhas Institute of Technology in New Delhi, India, as Assistant Professor. Currently he is working toward his Ph.D. at University of Genoa, Genoa, Italy. His research interests include interface electronics for tactile sensors, circuit simulations, measurements, analog electronics and transistor modeling.

He was awarded 3rd best paper of conference at ICM, Tunisia, in 2011, sponsored by IEEE. At present he has 8 papers in international journals and conferences.