Forward Body Biased Multimode Multi-Threshold CMOS Technique for Ground Bounce Noise Reduction in Static CMOS Adders

Shashikant Sharma, Anjan Kumar, Manisha Pattanaik, and Balwinder Raj

***Abstract*—As technology is continuously scaling down leakage current is increasing exponentially. Multi-Threshold CMOS technique is a well known way to reduce leakage current but it gives rise to a new problem i.e. ground bounce noise which reduces the reliability of the circuit and because of this circuit may incorrectly switch to the wrong value or may switch at the wrong time. Ground bouncing noise produced during sleep to active mode transitions is an important challenge in Multi-Threshold CMOS (MTCMOS) circuits. The effectiveness of noise-aware forward body biased multimode MTCMOS circuit techniques to deal with the ground bouncing noise is evaluated in this paper. An additional wait mode is investigated to gradually dump the charge stored on the virtual ground line to the real ground distribution network during the sleep to active mode transitions. The peak amplitude of the ground bouncing noise is reduced by 93.28% and standby leakage current is reduced by 23.94% as compared to standard trimode MTCMOS technique.**

To evaluate the significance of the proposed multimode Multi-Threshold CMOS technique, the simulation has been performed for 16-bit full adder circuit using BPTM 90nm standard CMOS technology at room temperature with supply voltage of 1V .

***Index Terms*—Forward body bias, ground bounce noise, leakage current, sleep to active mode transition.**

I. Introduction

As the dimension of MOSFET is continuously scaling down, the supply voltage of integrated circuits is also scaling down to maintain reliability of devices [1], [2]. In order to maintain a satisfactory performance at a lower supply voltage, the threshold voltage (*Vth*) of MOSFET is also scaling down. Low threshold voltage however leads to an exponential increase in subthreshold leakage current. This leakage current contributes significantly to the total power consumption of integrated circuits [3], [4]. For portable devices such as mobile phones and laptops with long idle periods, suppressing the subthreshold leakage currents is highly desirable to extend the battery lifetime. MTCMOS is one of the popular leakage power reduction strategies applicable to idle circuits [5]-[8]. In MTCMOS circuit, high threshold voltage (*high-|Vth|*) sleep transistors (header and footer) are used to cut off the power supply or the ground connection to the idle low threshold voltage (*low-Vth)* circuit blocks [9]. When MTCMOS circuit transits from the sleep to the active mode, sudden currents flow through the sleep transistors and large voltage fluctuations occur on both the real power line (power bouncing noise) and the real ground (ground bouncing noise) as illustrated in Fig. 1.

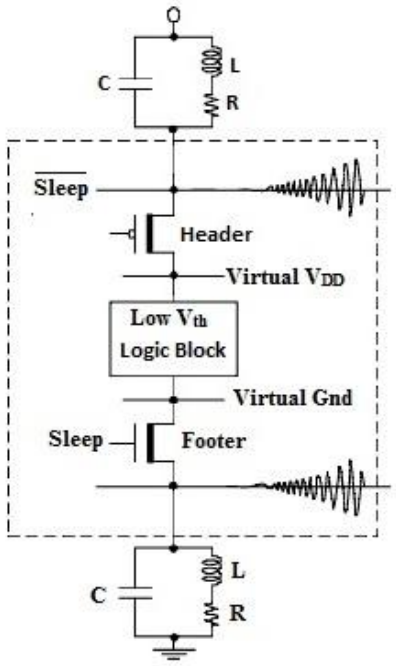

Fig. 1. Power and ground bouncing noise generated in conventional MTCMOS circuit.

This sudden voltage fluctuation is known as *Δi* noise, ground-bounce noise or simultaneous switching noise [10]-[12].Power and ground bouncing noise (activation noise) are expected to become increasingly important reliability issues in future deeply scaled MTCMOS integrated circuits with shrinking noise margins. Various MTCMOS techniques like trimode MTCMOS, dual-switch MTCMOS, tri-transistor controlled MTCMOS have been proposed in past for ground bounce noise and leakage current reduction [13]-[15]. Ground bouncing phenomenon in noise-aware Forward Body Biased (FBB) multimode Multi-Threshold CMOS circuits is evaluated in this paper. A novel FBB multimode Multi-Threshold CMOS structure is presented to effectively suppress the ground bouncing noise during mode transition (sleep to active mode transition) and leakage current during standby mode in gated ground MTCMOS circuits.

The paper is organized as follows: Ground bounce noise and leakage current aware FBB multimode MTCMOS technique has been proposed in Section II. Analysis of leakage current and ground bounce noise for proposed FBB

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multimode MTCMOS has been done in Section III. Experimental results are presented to characterize the noise-aware FBB multimode MTCMOS circuit techniques in Section IV. The paper is concluded in Section V.

II. Proposed FBB Multimode MTCMOS Technique

FBB multimode MTCMOS technique shown in Fig. 2 has been introduced in this section to further reduce the activation noise and standby leakage current.

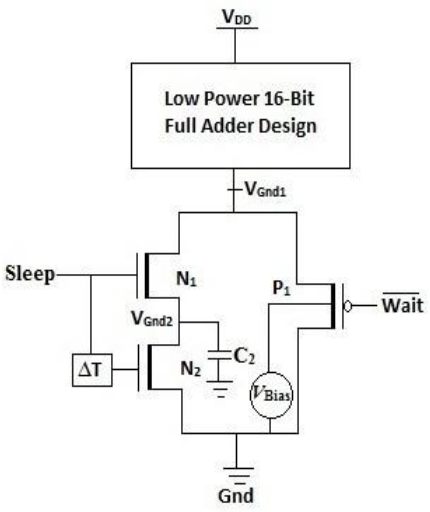

Fig. 2. FBB multimode multi-threshold CMOS technique.

In this technique high threshold sleep transistors (N_1, N_2, and P_1) are used to reduce leakage current effectively. Transistor stacking is an effective way to reduce leakage current so two high threshold NMOS transistors (N_1 and N_2) are used in stack. An additional wait mode is being introduced between sleep and active mode so that discharging of virtual ground voltage (V_{Gnd1}) during sleep to active mode can be divided into two parts using wait mode which will reduce peak of ground bounce noise efficiently. Delay ΔT is provided between the activation of two transistors (N_1 and N_2). This delay isolates the ground for a short period of time during the mode transition. An additional capacitor C_2 is inserted in the intermediate node V_{GND2} to control the drain current flowing through the second sleep transistor N_2 in mode transition. Forward body biasing voltage (V_{Bias}) has been applied to wait transistor so that more virtual ground voltage get discharged during sleep to wait mode transition. Detailed analysis has been done in Section III.

III. Analisis of FBB Multimode MTCMOS Technique

The proposed technique works on following two strategies.

A. Strategy for Standby Leakage Current Reduction

In this technique the leakage current is reduced by turning OFF transistors N_1, N_2 and P_1 in standby mode. The expression for the sub threshold leakage current is [3]:

$$I_{SUB} = Ae^{\frac{q}{nkT}(V_{gs}-V_{th0}+\gamma V_{bs}+\eta V_{vds})}(1-e^{\frac{-qV_{ds}}{kT}}) \quad (1)$$

$$A = \mu_n C_{ox}\frac{W}{L}(\frac{KT}{q})^2 e^{1.8}$$

V_{th0} is the zero bias threshold voltage, γ is the body effect coefficient and η is the DIBL coefficient, C_{ox} is the gate-oxide capacitance and μ_n is mobility. V_{gs}, V_{bs} and V_{ds} are the gate to source, bulk to source and drain to source voltages respectively. Equation (1) shows that the sub threshold leakage current will reduce exponentially if body effect is increased (negative V_{bs}) and drain-to-source voltage V_{ds} is decreased.

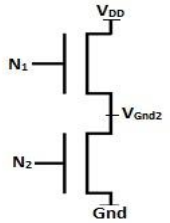

Fig. 3. Stacking structure (transistor N_1 and N_2).

In the stacking structure shown in Fig. 3 when sleep transistors are turned OFF in standby mode then the voltage of the intermediate node V_{GND2} raises to the positive values due to small drain current of the sleep transistor N_1. Further, due to this positive potential at the intermediate node the drain-to-source potential (V_{ds1}) of N_1 decreases resulting in less drain induced barrier lowering and negative body-to-source potential (V_{bs1}) of N_1 causes more body effect. This will reduce leakage current effectively.

B. Strategy to Reduce Peak of Ground Bounce noise During Mode transition

Ground bounce noise can be reduced by limiting the large transient current flowing through the sleep transistors during mode transition. When sleep transistor is turned ON, voltage of virtual ground goes down sharply causing fluctuations in ground rail. The voltage of the virtual ground line is maintained at V_{DD} during the sleep mode. Prior to the activation of the circuit, the P_1 transistor is turned on while transistor N_1 and N_2 is maintained in cut-off. The circuit transits to the intermediate wait mode. Forward body biasing [15] has been done for wait transistor so that threshold voltage of wait transistor can be reduced without increasing the width and more virtual ground voltage can discharge during first transition (from sleep to wait mode). The virtual ground line is discharged to the threshold voltage of the wait transistor V_{tp} and then transition from wait mode to active mode takes place. The ground bouncing noise is suppressed due to the lower range of the voltage swings on the virtual ground line with the two-step transition from the sleep mode to the active mode through the intermediate wait mode. To complete the reactivation process from wait to active mode, the stacked transistors N_1 and N_2 are subsequently turned on. The transistor P_1 is turned off. By isolating the ground for small duration during mode transition and turning ON the N_1 transistor in linear region instead of saturation region ground bounce noise will reduce effectively.

During wait to active mode transition, transistor N_1 is turned ON and transistor N_2 is turned ON after a small duration of time (ΔT). The logic circuit is isolated from the ground for a short duration as the transistor N_2 is turned OFF. During this time, the ground bounce noise can be greatly

reduced by controlling the intermediate node voltage V_{GND2} and operating the transistor N_1 in triode region.

The intermediate node (V_{GND2}) voltage can be controlled by

1) Inserting proper amount of delay, that is less than the discharging time of the N_1 transistor.
2) Proper selection of the capacitance C_2.

As we already know that, the voltage across the capacitor does not change instantaneously, the voltage across capacitors C_1 and C_2 remain same by instantaneously turning on the sleep transistor N_1. Now the equivalent circuit for stacked transistors during wait to active mode is shown in Fig. 4.

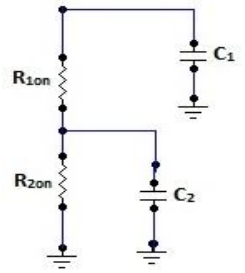

Fig. 4. Equivalent circuit for stacked transistors(N_1 and N_2) during wait to active mode transition.

Here R_{1ON} is the ON resistance of sleep transistor N_1, C_1 is the internal capacitance at virtual ground node V_{GND1} and C_2 is the external capacitance at intermediate node V_{GND2}.The voltage across the capacitor $C_1 \approx V_1$, and the voltage across the capacitor $C_2 \approx V_2$.

When $\Delta T > t > 0$, the capacitor C_1 having voltage V_1 will begin to discharge, and the capacitor C_2 will be charging by the amount with which C_1 is discharging. This process will continue until both the capacitances have the same potential. From above point of view by controlling the capacitor C_2 and ΔT we will be able to control the intermediate node voltage V_{GND2} so that both the transistors (N_1 and N_2) can be turned on in triode region and hence voltage swing at ground rail during wait to active mode transition can be controlled and ground bounce noise will reduce effectively.

C. Caluculation of ΔT Minimum

By turning on transistors N_1 and N_2 in the triode region peak of ground bounce noise can be reduced. ΔT_{min} is the minimum ΔT delay that has been provided to the transistor N_2, so that transistor N_1 can just enter in to triode region from saturation region and because of this transistor N_1 and N_2 turn ON in triode region.

If $\Delta T < \Delta T_{min}$, transistor N_2 turns ON in triode region but transistor N_1 turns ON in saturaion. Hence the stacking of sleep transistors is effective to reduce ground bounce noise only when $\Delta T \geq \Delta T_{min}$.

The condition for minimum ΔT is:

$$V_{GS1} - V_{TH} >= V_{DS1}$$

When $\Delta T > t > 0$,

$$V_{GS1} = V_{G1} - V_{S1}(t),\ V_{DS1} = V_{R1(ON)}(t) \quad (2)$$
$$V_{R1on}(t) = V_{C1}(t) - V_{C2}(t)$$
$$V_{G1} = V_{DD},\ V_{S1}(t) = V_{C2}(t)$$

so (2) can be simplified and written as:

$$V_{G1} - V_{S1}(t) - V_{TH} >= V_{R1ON}(t)$$
$$V_{DD} - V_{C2}(t) - V_{TH} >= V_{R1on}(t) \quad (3)$$

By further simplifying (2), the minimum ΔT is derived as [12] :

$$\Delta T_{\min} = \tau \ln[\frac{1}{\{1-[\frac{C_1+C_2}{C_2}](\frac{V_{TH}}{V_1})]\}}]$$
$$\tau = R_{1on}(\frac{C_1 C_2}{C_1 + C_2})$$

IV. Results and Discussion

The simulation setup has been done for low power 16 bit full adder, including ground bounce noise model with multimode technique. Here the effectiveness of noise-aware forward body biased multimode MTCMOS circuit techniques has been demonstrated using 16 bit full adder circuit for leakage current and ground bounce noise reduction. This is the very important block in any of the logic circuitry, so all the observations are made for this circuit topology.

Fig. 5 shows design of 1-bit full adder and by using this one bit full adder 16 bit full adder has been designed and is being taken as a Design Under Test (DUT). The CMOS structure is a combination of PMOS pull up and NMOS pull down networks to produce desired outputs. Transistor sizes are specified as a ratio of Width/Length (W/L). The sizing of transistors plays an important role in static CMOS style. The smallest transistor considered has a width of 120nm and length of 100nm and gives W/L ratio of 1.2 for 90nm technology. Fig. 6 shows design of 16 bit full adder design.

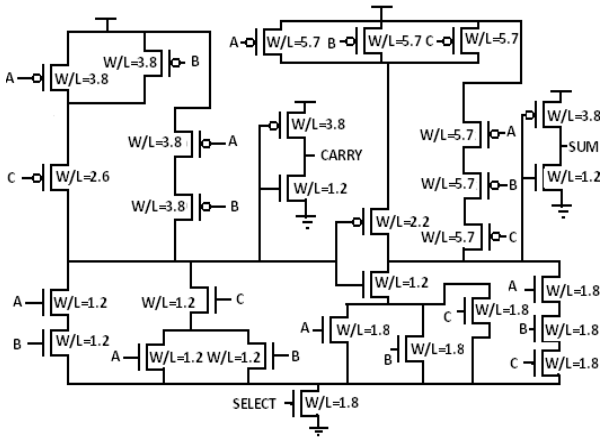

Fig. 5. Low power 1-bit full adder design.

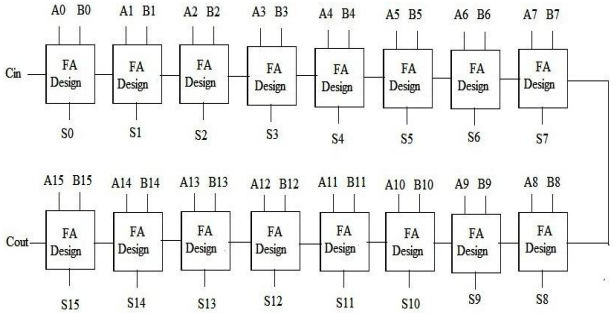

Fig. 6. Low power 16-bit full adder design.

The simulation has been using Tanner SpiceV13.0 simulator using BPTM 90nm technology with supply voltage of 1V at room temperature. For modeling ground bounce noise the electrical characteristics of DIP-40 package model has been used as shown in Fig. 7 [10].

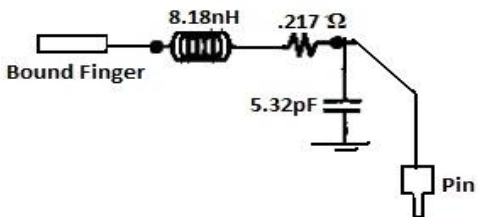

Fig. 7. DIP -40 package pin ground bounce noise model.

All the below mentioned results have been simulated under the condition that the all logical inputs of 16 bit full adder circuit are held at logic '1' for ground bounce noise calculation (worst case for peak ground bounce noise) and '0' for standby leakage current calculation (worst case for leakage current) and carry signal C_{in} is taken as '0'. To show the improvement in peak of ground bounce noise and standby leakage current FBB multimode MTCMOS circuit techniques has been compared with standard trimode MTCMOS technique (best for peak of ground bounce noise and standby leakage current reduction[13]-[14]) .

Table I shows effect of delay (ΔT) on ground bounce noise for proposed design when biasing voltage is 1V. It has been observed that ground bounce noise for a delay of .6nS is minimum because for this much of delay capacitor C_1 and C_2 discharges with equal voltage. As delay increases discharging of capacitor C_2 is more as compared to C_1 hence peak of ground bounce noise increases.

TABLE I: EFFECT OF DELAY (ΔT) ON PEAK OF GROUND BOUNCE NOISE

Delay ΔT (ns)	0	0.2	0.4	0.6	0.8	1
Peak of Ground Bounce Noise (mV)	22.3	17.95	17.66	17.63	18.05	18.48

The ground bounce noise produced for different wait transistor sizes by trimode and noise-aware forward body biased multimode MTCMOS circuit technique is characterized in Table II. In order to reduce peak of ground bounce noise with different wait transistor sizes an additional forward body bias voltage (V_{Bias}) have been used. V_{Bias} is swept from -200mV to -700mV for different wait transistor sizes and it has been calculated that for which biasing voltage ground bounce noise is minimum. It has been evaluated that for V_{Bias} = -600mV (V_{Bias_opt}) peak of ground bounce noise is minimum and ground bounce noise has been calculated for that biasing voltage (V_{Bias_opt}) for different wait transistor sizes.

The peak of ground bounce noise is minimized by adjusting forward body biasing voltage and wait transistor size. For proposed design, stacking of transistors and suitable wait transistor size with forward body biasing reduces peak of ground bounce noise effectively as shown in Fig. 9. Forward body biased multimode MTCMOS circuit with V_{Bias} = $V_{\text{Bias\_opt}}$ achieves minimum peak of ground bounce noise for wait transistor size of 3 µ m as shown in table II. It has been seen that for wait transistor size greater than 11µm instead of second peak, first peak of ground bounce noise starts dominating. When V_{Bias} = V_{Bias_opt} ground bounce noise for FBB multimode MTCMOS technique reduces by 93.28% as compared to standard trimode MTCMOS technique.

TABLE II: PEAK OF GROUND BOUNCE NOISE COMPARISON FOR 16-BIT FULL ADDER DESIGN DURING MODE TRANSITION

Wait Transistor Size (µm)	Trimode MTCMOS Technique (mV)[14]	FBB Multimode MTCMOS Technique (mV)
1	18.9	1.17
3	15.78	1.06
5	15.34	1.21
7	15.2	1.69
9	15.31	2.14
11	15.47	2.61
13	15.56	3.07
15	15.87	3.52

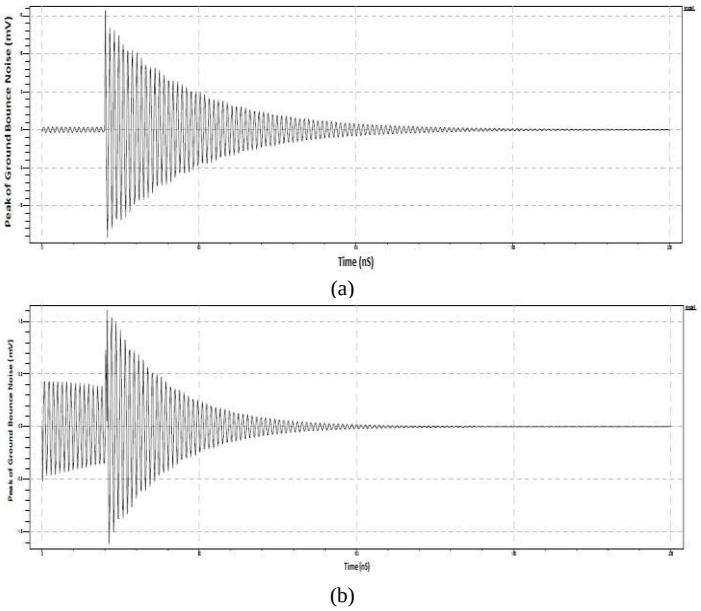

Fig. 8. Waveforms showing peak of ground bounce noise with time (nS) for wait transistor size 3 µm, V_{Bias}= -600mV, ΔT = .6nS (a) Standard trimode MTCMOS technique (b) proposed FBB multimode MTCMOS circuit technique.

Table III shows leakage current comparison of 16-bit full adder design for noise-aware forward body biased multimode MTCMOS technique and trimode MTCMOS technique. Fig. 10 shows stand by leakage current relation with supply voltage scaling. As supply voltage scales down leakage current in standby mode also reduces. It has been observed that for FBB multimode MTCMOS technique reduces leakage current by 23.94% as compared to standard trimode MTCMOS technique.

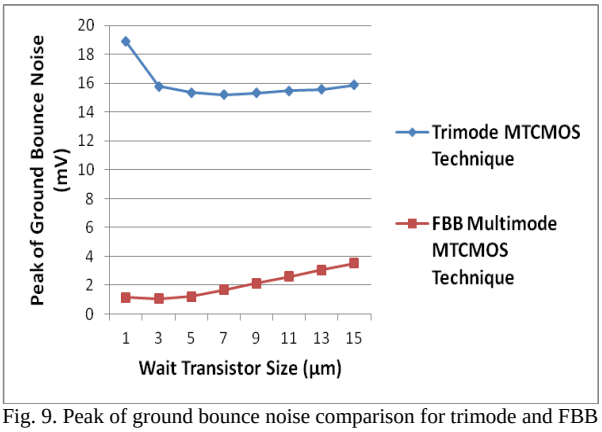

Fig. 9. Peak of ground bounce noise comparison for trimode and FBB multimode MTCMOS technique.

TABLE III: LEAKAGE CURRENT COMPARISON FOR 16-BIT FULL ADDER IN SLEEP MODE

Supply Voltage (V)	I_{Leak} Trimode MTCMOS Technique (nA) [14]	I_{Leak} FBB Multimode MTCMOS Technique (nA)
1	3.80	3.16
.9	3.36	2.74
.8	2.98	2.39
.7	2.66	2.09
.6	2.38	1.84
.5	2.13	1.62

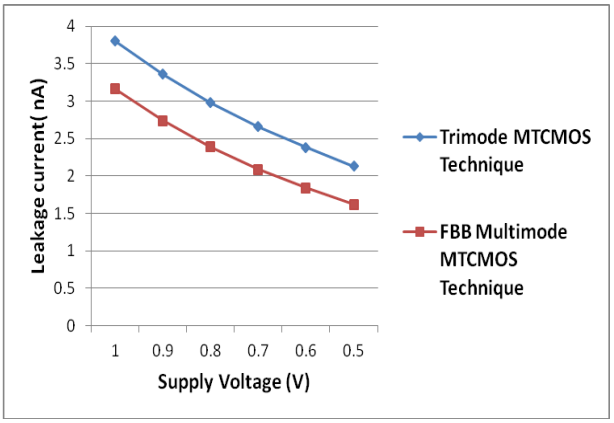

Fig. 10. Leakage current versus supply voltage scaling with trimode and FBB multimode mtcmos technique.

V. CONCLUSION

A high performance forward body biased multimode MTCMOS technique has been presented which reduces peak of ground bounce noise during mode transition and leakage current in standby mode. Effect of stacking and multimode with forward body biasing on leakage current and ground bounce noise has been evaluated in this paper. It has been seen that in proposed design for delay (ΔT) of .6ns ground bounce noise is minimum that is 17.63mV. It has been observed that for different wait transistor sizes for -600mv body bias voltage peak of ground bounce noise is minimum.

It has been evaluated that forward body biased multimode MTCMOS technique reduces peak of ground bounce noise by 93.28% and reduces standby leakage current by 23.94% as compared to standard trimode MTCMOS technique.

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