A 10 GHz Low Phase Noise Split-Ring Resonator Oscillator

Nor Muzlifah Mahyuddin and Nur Liyana Abdul Latif

***Abstract*—In this project, a method of designing a series feedback split ring resonator (SRRs) oscillator with emphasize on phase noise study has been proposed. The split ring resonator oscillator is consisted of an active device of ATF-36077, a GaAs PHEMT from Agilent, an array of split ring resonator for frequency determining element and microstrip-based output matching network. Mainly, this work focused on modeling and designing an optimum performance of SRRs oscillator in emphasizing the phase noise result. The simulation of SRRs oscillator has been modeled using Agilent Advanced Design System (ADS) and CST Microwave Studio software. Three designs of SRRs have been compared for Q-factor in which a high Q-factor of 6476 has been obtained from File C of SRR design. Subsequently, based on this design, the oscillator exhibited a low phase noise of -122.0 dBc/Hz at offset frequency of 100 kHz and an output power of 7.46 dBm at the oscillating frequency of 10.05GHz.**

***Index Terms*—Low phase noise, oscillator, quality factor, split-ring resonator.**

I. Introduction

The current exponential growth in wireless communication system also has increased the demand of more frequency bands with the emergence of new standards. The implementation of resonator using the microstrip line has attracted a lot of attention due to its simplicity. One of the applications is incorporating this resonator into an oscillator design. As it is well known, Q factor of the resonator determine the phase noise dominantly. Thus microstrip based resonators are incorporated with the microwave FET to generate oscillation. Designing a low phase noise oscillator is important because noise produced by an oscillator or other signal source may severely degrade the performance of a radar or communication receiver system. Therefore, a huge amount of effort has been invested to reduce the phase noise.

Microstrip-based resonator has been known for its limitation for reducing the phase noise because of the low Q-factor. However, split ring resonators (SRRs) have the ability to provide higher Q-factor based on its narrowband band-stop characteristics and metamaterial property. In addition, SRRs also provide easy fabrication, low radiation loss, high frequency stability and sharp selectivity in desired resonant frequency [1]. By adding more rings of SRRs, higher Q-factor can be achieved easily without the requirement to re-design the existing design [2]. SRRs are a cost effective solution for achieving a highly stable and low phase noise in the RF oscillator.

Therefore, in this paper a 10 GHz split-ring resonator oscillator incorporating different designs of SRR will be designed, compared and analyzed using two simulation tools, i.e. CST Microwave Studio and Agilent ADS.

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II. Split-Ring Resonator Design

In designing a split-ring resonator oscillator, the design will start off with the modelling of a split-ring resonator array, follows by an optimization process in which three SRR designs are compared in terms of insertion loss, return loss and Q-factor.

A. Split-Ring Resonator Modelling

SRRs commonly known as metamaterial structure are resonators that have split in the opposite ends of each concentric annular ring. The ring is commonly designed in array which have small gap between them. The gaps of the inner and the outer rings are the main features in designing the SRR. It represents the capacitance of the rings while the inductance is represented by the area of both inner and outer rings [3]. In addition, the gaps with the total length of SRR also control the resonance frequency. Fig. 1 shows the schematic diagram of a single split-ring resonator with its parameters. These parameters are tabulated in Table I indicating the equations used to calculate these parameters.

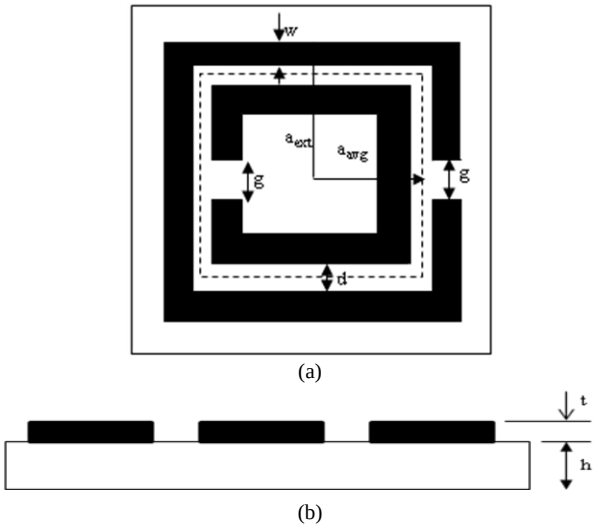

Fig. 1. Schematic view of (a) a square SRR formed with metallic strips of width, *w*, outer length, a_{ext}, and inner length, a_{avg} with inter ring spacing, *d* and split gap, *g*. (b) with thickness of metallic strip, *t*, printed on dielectric substrate having thickness, *h*.

TABLE I: SRR DIMENSION AND PARAMETERS [4]

Parameter	Definition
f_o	Resonant frequency $\frac{1}{2\Pi\sqrt{L_T C_{eq}}}$
L_T	Total equivalent inductance for a wire of rectangular cross section of a single SRR having finite length, l and width, w $0.0002l\left(2.303\log_{10}\frac{4l}{w}-\gamma\right)\mu H$ $l = 8a_{ext} - g$
γ	Constant for a wire loop of square geometry, 2.853
C_{eq}	Total equivalent capacitance with series capacitance, C_o and gap capacitance, C_g $\frac{C_o + C_g}{2}$
C_o	$\left(4a_{avg} - g\right)C_{pul}$
a_{avg}	$a_{ext} - w - d/2$
C_{pul}	Capacitance per unit length $\sqrt{\varepsilon_T}/C_o Z_o$
Z_o	Characteristic impedance, 50Ω
c_o	Velocity of light in free space, $3X10^8$
C_g	$\frac{\varepsilon_o wt}{g}$

Referring to Volkan Oznazl and Vakur B. Erturk [5], the microstrip line will have higher Q factor and act as a bandstop filters when it is loaded with the SRR. This also indicates that better performance will be realized when SRR is in array coupling to the microstrip transmission line, as shown in Fig.2 which shows additional parameters, i.e. the width of the transmission line, c and the coupling gap between the transmission line and the SRR, c_p.

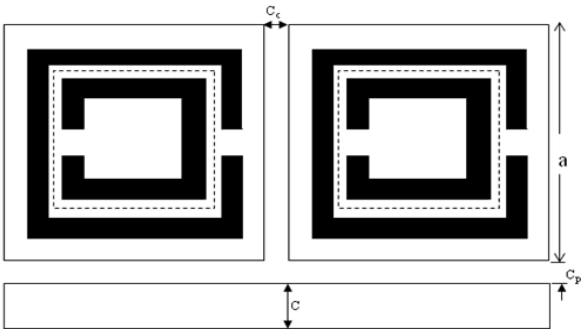

Fig. 2. Schematic view of a square SRR coupled to microstrip line with the width, c and the gap of c_p.

For this work, the SRR design is implemented in a 3D software called CST Microwave Studio (MWS) in which the coupling gap between the microstrip line and the SRRs is analyzed and optimized to meet the resonator requirement. Since only passive device can be implemented in CST MWS, another tool called ADS from Agilent is used for oscillator design.

The SRR array is modeled together with the RO4003C substrate and a 50 Ω microstrip line. The substrate has a thickness of 0.813 mm and a dielectric constant of 3.38. Fig.3 shows the side view of SRR modeling in CST MWS, as well as the dimension of a 50Ω transmission line with a width of 1.8653 mm and length of 30 mm.

The model design structures split ring resonators with one microstrip line with width and length calculated using LineCalc of ADS. For substrate in this design, it has been laminated with copper layer at both sides. The copper layer has an electrical conductivity of 5.9E+007 S/M and a height of 0.035 mm.

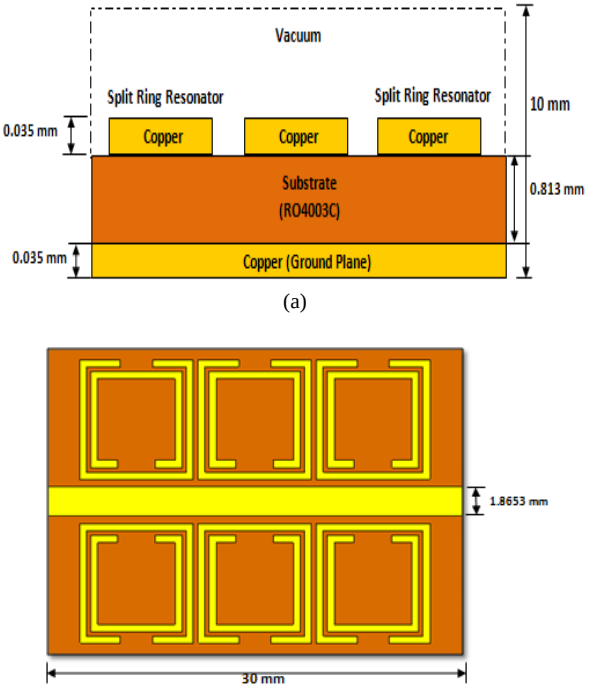

Fig. 3. (a) Side view of SRR modelling in CST MWS with (b) dimension of SRR array.

B. Comparison Analysis of SRR Designs

There are three designs of SRR that produce the best results. Table II shows the parameters used in each of the three files. Categorized as File A, File B, and File C, their response and parameters are slightly different from each other. The parameters can be referred to Fig. 1 and Fig. 2, and they are measured in mm. The difference between each of the three designs can be clearly seen in Table II. By comparing File A and File B, only the coupling gap between the adjacent rings, C_c is different. Meanwhile, the comparison between File B and File C indicates only difference in the number of rings. File B has 2 rings whereas File C has 3 rings in the SRR.

TABLE II: THREE DESIGNS OF SRR WITH PARAMETERS

	Definition of Parameters	File A	File B	File C
a	The length of the side of the square ($2*a_{ext}$)	8.1589	8.1589	8.1589
w	Width of the conductor	0.5	0.5	0.5
d	The dielectric width between the inner and the outer ring	0.5	0.3	0.3
g	Gap available in the rings	2.3	2.3	2.3
C_p	Coupling gap between rings and transmission line	0.3	0.5	0.5
C_r	Coupling gap between the adjacent rings	0.5	0.35	0.35
#	Number of rings in SRR	2	2	3

It can be seen from the results in Fig. 4 that the resonant frequency for the split ring resonator model occurs at approximately 10 GHz. The coupling between the microstrip transmission line and the split ring resonator structure is generated by orienting the magnetic momentum of the split

ring resonator perpendicular to the microstrip transmission line at an optimum distance.

From the S-parameter results in Fig. 4, the resonant frequency is acquired by looking at the frequency point where the port 2 insertion loss, S(2, 1) dips down the most. It is adequate to just consider S(2, 1) the insertion loss at port 2 for the model because it is reciprocal to S(1, 2) the insertion loss of port 1.

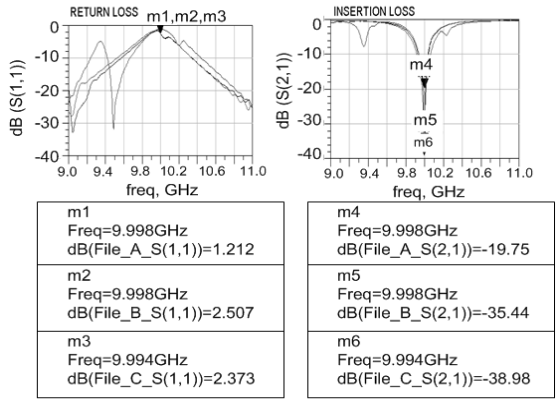

Fig. 4. Comparison results of File A, File B and File C.

From Fig. 4, File C shows the best result with the S(2,1) value of -38.98 dB and S(1,1) of -2.37 dB at 10 GHz. The better response for File C compared to File A and File B is due to File C having the most optimum coupling gap with the neighboring SRRs which is at 0.35 mm but the most important parameters that could have affect the performance is the increase in number of rings for File C. It has been noted that multiple ring SRR is better than double or single ring SRR, thus with the use of three rings SRR produces stronger coupling between the microstrip line and the SRR. It is known that stronger coupling reflects on higher Q-factor. This is shown in Table III where File C has a higher Q-factor when the three designs are compared. At this value of coupling gap and accommodating three rings of SRR, produce the best SRR performance.

TABLE III: THE Q-FACTOR COMPARISON BETWEEN THREE FILES

	File A	File B	File C
Q-factor	266.27	2950.11	6476.54

III. SPLIT RING RESONATOR OSCILLATOR DESIGN

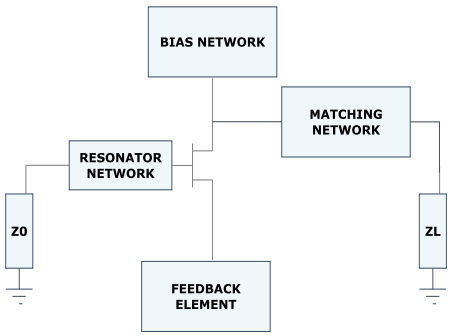

Fig. 5. Basic oscillator model.

Split ring resonator oscillator consists of active device, a resonator at operating frequency, RF choke network, DC bias circuit and output matching network. The common source series feedback topology is being selected for SRR oscillator. It consists of a resonator network, a feedback element, a biasing network, and a matching network as shown in Fig. 5.

The split ring resonator oscillator is designed to make the resistance generated by the feedback element negative enough to compensate the loss generated by the resonator. By rule of thumb, in a series circuit at least 1.2 times of the load resistance is required by the negative resistance to satisfy the start-up condition for the oscillator [6].

The important components for this oscillator design is the resonator, RF choke network, DC bias circuit and output matching network. Since the design of SRR has been previously explained in great details, the following sections will focus on the latter three components.

A. RF Frequency Choke Network

An oscillator consists of Radio Frequency choke or RF choke, which can be defined as a low pass filter since it is able to block a high frequency. The RF choke blocks AC signals specifically within a certain frequency band from propagating on DC signal paths. In other word, the DC voltage is supplied to the active device, at the same time it blocks the RF signal generated by an active device from going to the power supply circuit. If the RF leaks to the power supply circuit, it will reduce the gain and produce instability of the output frequency.

The RF choke network model is shown in Fig.6. The length of microstrip line between the 50 Ω transmission line and the radial stub require a 100 Ω transmission line measured at quarter-wavelength as calculated using Equ.1 below.

$$\lambda_g = \frac{c}{f\sqrt{\varepsilon_r}} \quad (1)$$

where,

λ_g = Wavelength of waveguide (m)
c = Speed of light (m/s)
f = Operating frequency (Hz)= 10 GHz
ε_r = Dielectric constant = 3.38

At the speed of light and operating frequency of 10 GHz with the dielectric constant of substrate is 3.38, the calculated wavelength is 16.32 mm which will give the quarter wavelength value of 4.08 mm.

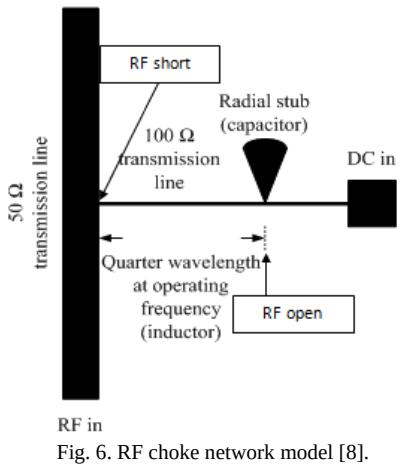

Fig. 6. RF choke network model [8].

Meanwhile the radial stub will act as a capacitor to

complete AC grounding [7]. After radial stub, there is another line from the radial stub to the DC in. It is noted that the length between radial stub and the DC bias voltage port can be set to any value. The RF choke network designed for this oscillator is as shown in Fig. 7.

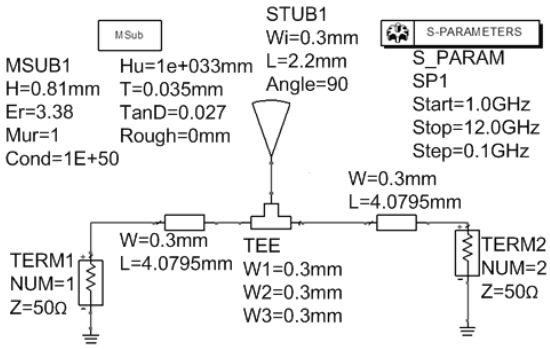

Fig. 7. Schematic of RF choke network with quarter wavelength.

B. DC Bias Circuit

The oscillator design as stated in Fig.5 indicates that the oscillator is biased by power supply to the active device in order to operate. However, this design only requires one power supply, $V_{DD.}$ By referring to the datasheet of ATF 36077[9] when V_{DD} is 3V, I_D is 10 mA, V_{DS} is 1.5 V, R_D is calculated using Equ.2, which equals to 150 Ω.

$$V_{DD} = I_{DD} R_{DD} + V_{DS} \tag{2}$$

To avoid DC supply from providing admittance to the radio frequency, a DC blocking capacitor, C_B is placed in series before output terminal. At 10 GHz, the value of this capacitor can be calculated using Equ.3 where $w = 2\pi f$ which gives the value of 15.9pF.

$$\frac{1}{wC_O} = 1\Omega \tag{3}$$

The DC block capacitor usually ranges from 1 pF to 100 pF. The smaller the capacitance, the more effective the DC supply is blocked [8]. Since the value of C_B is 15.9 pF, so the actual value for C_B must be less than 15.9 pF. In this work, a 1 pF capacitor has been chosen in the split ring resonator oscillator circuit design.

C. Output Matching Network

Output matching for this work is included to stabilize the circuit and provide an additional gain. The matching networks are tuned or optimized until the desired result is achieved. Such step will ensure maximum reflection at the load looking into the oscillator output circuit. It is crucial to ensure that 50 Ω lies in the unstable region by looking at the instability circle of the oscillator. As a result, a small negative resistance at the oscillator port will occur. The most preliminary step in output matching is verifying the transistor ATF-36077 used in this work is unstable by calculating the stability factor, *K* [10]:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{1|S_{12}||S_{21}|} \tag{4}$$

Therefore from the computation value of K=-0.664 which is less than 1 (<1), indicates potentially unstable performance of transistor [10]

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$$\frac{1}{\Gamma_T} = \Gamma_{OUT} = S_{22} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{11}\Gamma_L} \tag{5}$$

$$Z_{OUT} = Z_0 \frac{1 + \Gamma_{OUT}}{1 - \Gamma_{OUT}} \tag{6}$$

$$Z_T = \frac{-R_{OUT}}{3} - jX_{OUT} \tag{7}$$

$$\Gamma_T = \frac{Z_T - Z_0}{Z_T + Z_0} \tag{8}$$

From all equations above, Γ_T is calculated to be $0.97\angle$-49.34° by plotting in the Smith Chart, the distance of open stub to the active device is 2.61 mm and length of stub is 4.44 mm. Upon designing all the components needed in SRR oscillator, the final design of SRR oscillator is modelled in ADS as shown in Fig.8. The Touchstone file from CST MWS containing the SRR design is incorporated into the oscillator design.

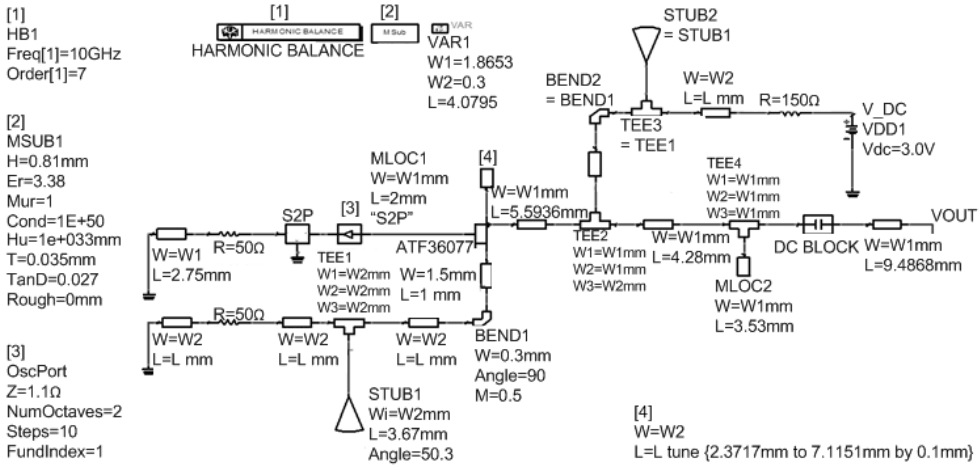

Fig. 8. Split-ring resonator oscillator design in ADS.

IV. Results and Discussion

Previously, three designs of SRR have been compared in terms of insertion loss, return loss and Q-factor. File C shows better performance overall as it has better coupling gap value and more number of rings in SRR compared to other designs.

In order to compare the oscillator performance incorporating all three SRR designs, the Touchstone files from CST MWS for File A, File B and File C are incorporated into the oscillator design in ADS. The design metric of interest for oscillator are the phase noise and the output power at the oscillating frequency of 10GHz.

The results of SRR oscillator are compared and analyzed. Fig.9 shows the results of simulation for SRR Oscillator using Touchstone files from File A, File B and File C. All three results are also tabulated in Table IV for comparison.

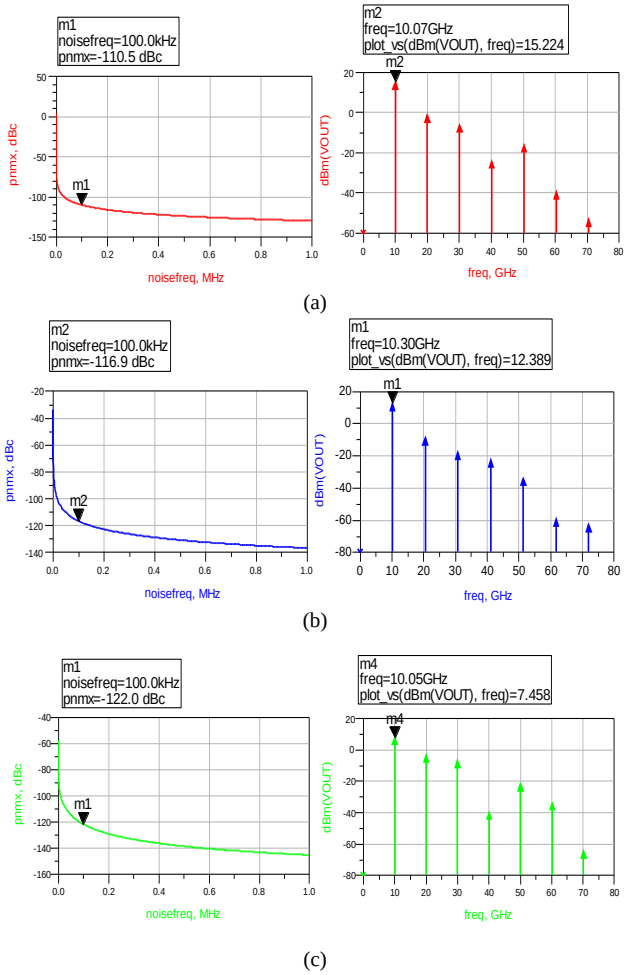

Fig. 9. Result for SRR oscillator for (a) File A (b) File B and (c) File C.

TABLE IV: Comparison between Oscillators Using File A, File B and File C SRR Design

	File A	File B	File C
Phase Noise (dBc/Hz)	-110.50	-116.90	-122.00
Output Power (dBm)	15.22	12.39	7.46
Oscillating Frequency (GHz)	10.07	10.30	10.05

By comparing all the phase noises from the results above, File C give the best phase noise performance compared to the other two designs. These outcomes verify that higher Q-factor will result in lower phase noise. Subsequently, other parameters that can influence the SRR performance are the dielectric width between the inner and outer ring, *d*, and the coupling gap between the adjacent rings, C_c.

V. Conclusion

In this work, a split ring resonator has been designed and being applied in the design of a series-feedback common source Split Ring Resonator oscillator that operate in X-band. This oscillator topology is applied with the concept of negative resistance. The SRR provides a sharp hard-rejection characteristic and high quality factor, providing a stop-band characteristic.

In the resonator design part, varying the characteristics of the resonator such as coupling gap with the microstrip line, coupling gap with the neighboring SRR and the number of rings in individual SRR give the variations in the Q-factor, indirectly affecting the phase noise performance of the oscillator. This work indicates that the SRR design with the highest Q-factor when implemented into the oscillator design produces the output power of 7.46 dBm at 10.05 GHz which is acceptable as it is less than 1% vary from the required oscillating frequency. In addition, the phase noise exhibited -122.0 dBc/Hz at a frequency offset of 100 kHz. Thus, at a phase noise of -122.0dBc/Hz, the minimum low phase noise split-ring resonator oscillator is successfully designed.

In addition, the SRRs structure that being implemented in this work also presents the advantages of low cost, low loss, small size and easy fabrication for planar integration of active device and bias circuit.

References

[1] J. Jinse, C. Choon Sik, J. W. Lee, K. Jaeheung, and H. Tae, "A low phase noise microwave oscillator using split ring resonators," presented at the 36th European Microwave Conf., pp. 95-98, 2006.

[2] C. Jaewon and S. Chulhun, "Microstrip Square Open-Loop Multiple Split-Ring Resonator for Low-Phase-Noise VCO," *IEEE Trans. Microwave Theory and Techniques*, vol. 56, pp. 3245-3252, 2008.

[3] M. R. Vidyalakshmi and S. Raghavan, "A cad model of triangular split ring resonator based on equivalent circuit approach," presented at Applied Electromagnetics Conference (AEMC), pp. 1-4, 2009.

[4] C. Saha *et al.*, "Square split ring resonator backed coplanar waveguide for filter applications," presented at General Assembly and Scientific Symposium, pp. 1-4, 2011.

[5] V. Öznazl and V. B. Erturk. (August 2013). On the use of Split-ring Resonators and Complementary Split-ring Resonators for Novel Printed Microwave Elements: Simulations. *Experiments and Discussions.* [Online]. Available: www.emo.org.tr/ekler/0a7476842882400_ek.pdf

[6] Jinawan, "Design of a 5.305 GHz dielectric resonator oscillator with simulation and optimization," *J. Electronic Science and Technology of China*, vol. 6. pp. 342, 2008.

[7] M. F. Ain, "Superconducting oscillators," Ph.D. dissertation, Univ. of Birmingham, Birmingham, UK, 2003.

[8] N. M. Mahyuddin, M. F. Ain, S. I. S. Hassan, and M. Singh, "Modeling of a 10GHz dielectric resonator oscillator in ADS," presented at IEEE Int. RF and Microwave Conference, pp. 106-110, 2006.

[9] ATF36077 Datasheet. (February 2013). [Online]. Available: www.avagotech.com/docs/AV02-1222EN

[10] D. M. Pozar, *Microwave Engineering*, Canada: John Wiley & Sons, 2005.

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