Design of CMOS Crystal Oscillator with Low Power Consumption

Qichao Zha, Tiejun Lu, Yu Zong, Jianhui Zhang, and Shaoxian Qu

***Abstract*—This work proposes a method to reduce the power consumption of Pierce crystal oscillator. This method is base on the mechanism of decreasing the clock signal amplitude. The circuit proposed in paper is designed based on XFAB 0.35μm CMOS technology to produce a 32768Hz clock signal. It operate over a supply voltage range 1.8V to 3.6V , a temperature range from -45 to 80℃. Spectre simulation results indicate that the current consumption of the crystal oscillator is only 254nA at 3V supply voltages and 27℃ temperature. Performance of the crystal oscillator in corner simulations is also observed. This low power consumption oscillator will greatly extend the life of consumer electronics.**

***Index Terms*—Pierce crystal oscillator, decrease amplitude, low power consumption.**

I. Introduction

Crystal oscillators are widely used to generate accurate reference frequency in electronic systems. However, constant frequency comes at the expense of higher power consumption and thereby affecting the life of battery, especially in low-power micro-controllerunit(MCU) and watch system. This issue is extremely important in the node of electronic system in mobile society.

Low power CMOS crystal oscillators have either been optimized for low current or for have low supply voltage [1]. But in most cases, low supply voltage can not satisfy with applications, on the other hand LDO additional will also cause the additional current. So the most important point for a low current consumption is an amplitude control, which reduces the supply current as soon as the oscillator amplitude reaches a reasonable value.

Therefore, some low power crystal oscillator circuit structure by this mechanism was reported [2]. This paper will present a new circuit with reducing the amplitude of oscillator to decrease the current consumption, and show the result of power improvement between the conventional circuit and circuit proposed in paper.

II. Pierce Crystal Oscillator

A. Conventional Crystal Oscillator Circuit

The conventional crystal oscillator circuit widely used in electronic system is based on structure of pierce. The schematic is shown in the Fig. 1.

The conventional pierce crystal oscillator consists of two parts [3]. One is an inverting amplifier thatsupplies a voltage gain and 180 degree phase shift. The other is a frequency selective feedback path, which is out of the chip. The crystal combined with C1 and C2 to form a feedback network that tends to stabilize the frequency and supply 180 degree phase shift to the feedback path because of the π network. These conditions conform with the Barkhausen criterion of oscillation that overall phase shifts is zero and a closed loop gain should be over or equalto one.

The feedback resistance Rf, is used to bias the inverting amplifier to stabilize the static operating point of amplifier. Generally the feedback resistance doesn't require precise resistor but large numerical value. And so we can use large length and small width transistor instead of Rf.

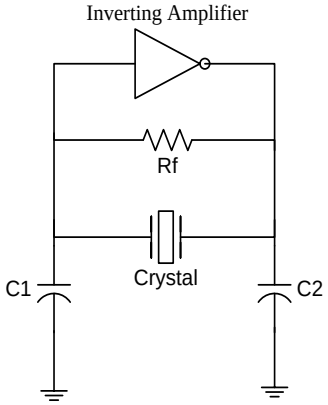

Fig. 1. Schematic of conventional pierce crystal oscillator.

B. Crystal Model

Crystal is the main component of generating oscillation clock signal. However, in simulation we only use its equivalent circuit instead of a crystal.

Fig. 2 shows the equivalent circuit of crystal. R is the effective series resistance in the crystal, as well as L and Cs are the motional inductance and capacitance of the crystal. Cp is the parasitic shunt capacitance due to the electrodes. In parallel resonant mode, the crystal will look and perform like a low resistance.

For generating 32.768kHz signal, we set L =47.22H, Cs=0.5pF, Cp=100pF.

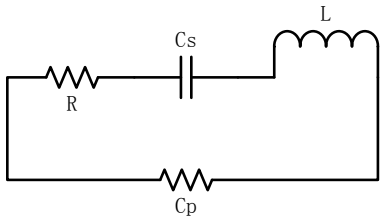

Fig. 2. The equivalent circuit of crystal.

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When the crystal is operating at series resonance, it looks purely resistive and the series resonance frequency is given by

$$f_s = \frac{1}{2\pi\sqrt{LC_S}}$$

When the crystal is operating at parallel resonance, it looks inductive. And the parallel resonance frequency is given by

$$f_s = \frac{1}{2\pi\sqrt{L\frac{C_S C_p}{C_S + C_p}}}$$

These frequencies satisfy with the frequency 32.768kHz needed in simulation.

III. New Circuit Proposed

Generally, the inverting amplifier in pierce crystal oscillator circuit is used by a common inverter. In CMOS technology, the dynamic power consumption caused by the capacity charging and discharging account a large part of total.

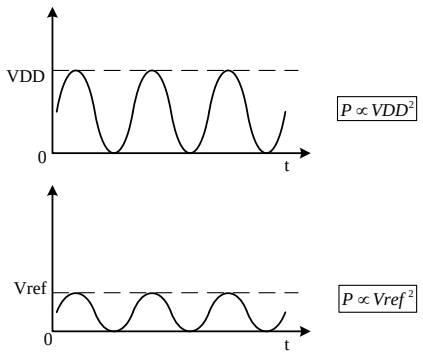

Fig. 3. The relationship of power and amplitude.

The relationship of power and amplitude is shown in Fig. 3. For the quadratic relationship, decreasing the amplitude of oscillator becomes a efficacious mean to reduce the power consumption in oscillator circuit. But the power consumption of additional circuit module for decreasing the amplitude shouldn't be high.

The proposed crystal oscillator circuit is shown in Fig.4, which includes voltage reference circuit, pierce circuit and Level shift circuit.

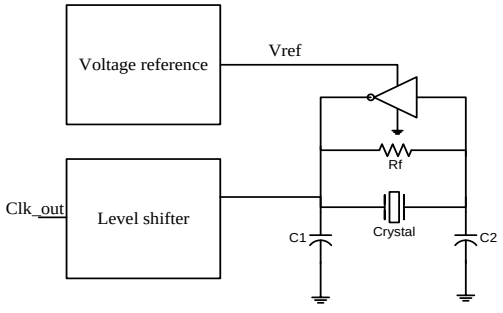

Fig. 4. Block diagram of crystal oscillator proposed in paper.

A. Pierce Circuit

In the pierce circuit，we add the current limiting resistance R1 and R2 to both ends of inverting amplifier. We maintain the other part of pierce with the conventional circuit.

B. Voltage Reference Circuit

Voltage reference circuit determines the voltage of vref to result in the sine wave generate from crystal. The principle of it is illustrated in Fig. 5. The circuit consists of a current source subcircuit and a bias-voltage subcircuit. The current source subcircuit is a modified β multiplier self-biasing circuit that uses a MOS resistor MR instead of ordinary resistor. The bias-voltage subcircuit consists of a transistor (M7) and two source-coupled pairs (M6-M9 and M8-M10). The gate-source voltages of M3 and M7 in the bias voltage subcircuit and MR in the current source subcircuit form a closed loop [4].

All the MOSFETS in bias-voltage subcircuit and current source subcircuit except for MR are operated in thesubthreshold region for nA-level current consumption.

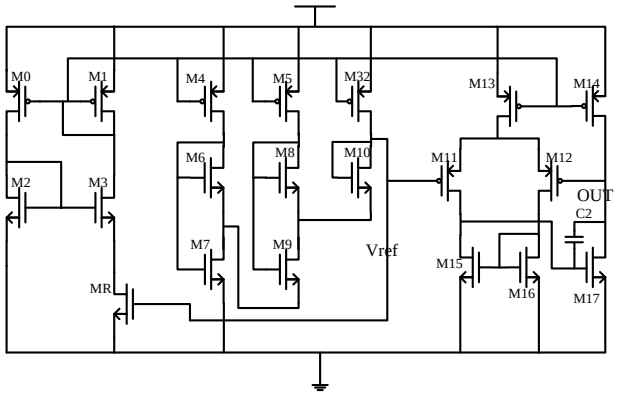

Fig. 5. The voltage reference circuit.

The subthreshold drain current of a MOSFET is an exponential function of the gate-source voltage Vgs and the drain-source Vds. The function is shown in equation (1).

$$I_d = \frac{W}{L} I_0 \exp\left(\frac{V_{GS}-V_{TH}}{\eta V_T}\right) \times (1 - \exp(-\frac{V_{DS}}{V_T})) \quad (1)$$

$$I_0 = \mu C_{ox}(\eta - 1)V_T^2 \quad (2)$$

where μ is the carrier mobility,Cox is the gate-oxide capacitance, Vt is the thermal voltage and η is the subthreshold slope factor. For Vds> 0.1V, current Id is almost independent of Vds and given by

$$I_d = K \times I_0 \exp\left(\frac{V_{GS}-V_{TH}}{\eta V_T}\right) \quad (3)$$

MOSFETS M0, M1, M4, M5 and M32 make up the current mirror. And the value of each current branch is given by equation (4).

$$I_P = \frac{V_{DSR1}}{R_{MR}} = \frac{V_{GS2} - V_{GS3}}{\frac{1}{K_{MR}\mu C_{ox}(V_{ref}-V_{TH})}} = K_{MR}\mu C_{ox}(V_{ref} - V_{TH})\eta V_T \, ln\left(\frac{K_3}{K_2}\right) \quad (4)$$

Therefore, we find that voltage of Vref of the circuit is given by equation (5). $\kappa$is the temperature coefficient of V_{TH}.

$$\begin{aligned} V_{ref} &= V_{GS7} - V_{GS6} + V_{GS9} - V_{GS8} + V_{GS10} \\ &= V_{GS7} + \eta V_T \, ln\left(\frac{2K_6K_8}{K_9K_{10}}\right) \\ &= V_{TH} + \eta V_T \, ln\left(\frac{3I_P}{K_4I_0}\right) + \eta V_T \, ln\left(\frac{2K_6K_8}{K_9K_{10}}\right) \\ &= V_{TH0} - \kappa T + \eta V_T \, ln\left(\frac{3I_P}{K_4I_0}\right) + \eta V_T \, ln\left(\frac{2K_6K_8}{K_9K_{10}}\right) \end{aligned} \quad (5)$$

The transistor M11 and M12 compose of a differential operational amplifier make sure that the voltage of point OUT is equal to *V*ref. To ensure the close loop working stably , we need a capacity C2 play a role of Miler capacity in the structure of two stage amplifier.

C. *Level Shifter Circuit*

The Level shift circuit make the signal amplitude from 0~*V*ref get back to 0~VDD.

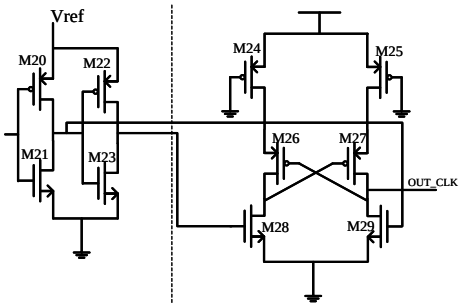

Fig. 6. The level shifter circuit.

Fig. 6 shows the circuit of level shifter. Two inverters play a role for signal shaping, the other play a role. Transistor M24 and M25 acts as great resistances for cutting down the current.The cross-linked MOSFETs M27 and M26 ensure no Static current exist in the two branches.

IV. Conclusion

We accomplished the simulations by spectre and Fig 7 and 8 show the transient current consumption wave of conventional circuit and proposed circuit in paper in common supply voltage(3V), temperature(27˚C) and corner (tm). The reason for existing positive current (in red current wave) is that the energy storage of inductance in crystal model causes the sink current.

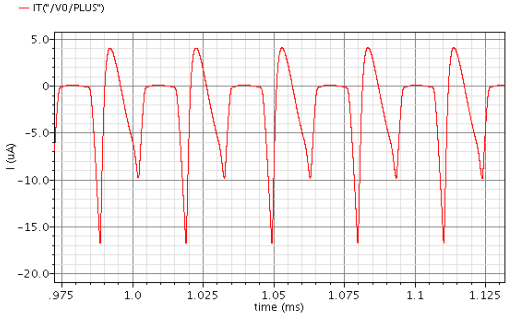

Fig. 7. Current consumption of conventional circuit with normal amplitude (2.3 μ A).

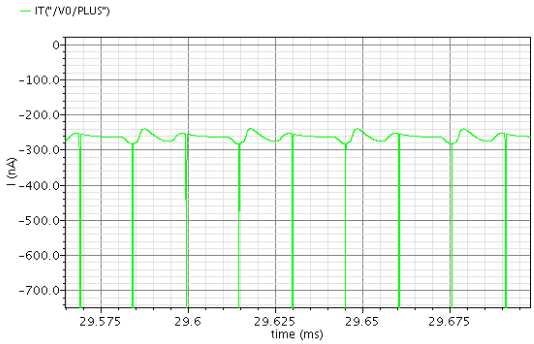

Fig. 8. Current consumption of proposed circuit with decreasing amplitude (254nA).

Compared the average currentcalculated in these two figures, the average current consumption ofconventional circuit with no decreasing amplitude is 2.3 μ A, but only 254nA in the proposed circuit with decreasing amplitude. It illustrates that power has been significantly improved with this method.

TABLE I: Current Consumption in Different Conditions

Corner	VDD supply(V)	Temperature(° C)	Current consumption（nA）
Tm(tt)	3	27	254.2
		85	241.5
		-40	289.4
	1.8	27	237.7
		85	207.6
		-40	217.9
Wp(ss)	3.6	95	285.0
		-40	350.0

Table I shows the current consumption in differentconditions, we can find that the maximum of current is350nA and the minimum is only 207.6nA.These low power consumption is sufficient to ensure long battery life. In Table 1,tm corner represents that the nmos and pmos are in typical corner,but worst power corner(wp) means that the nmos and pmos are in slow corner.

Comparison between different low power crystal oscillator Table II show the comparison of performance parametersreported in some low power crystal oscillators.

TABLE II: Comparison of Reported Low Power Crystal Oscillator

	This work	[5]	[6]	[7]
Process（μ m）	0.35	0.35		0.35
VDD（V）	1.8~3.6	1.6~3.6	1.8~3.5	
Temp(℃)	-40~85	-10~60	-10~70	
Current	254nA	102.1μA	500nA	390nA
Frequency(Hz)	32.768k	32.768k	2.1M	32.768k

In conclusion it can be said that decreasing amplitude in crystal oscillator is an effective means of reducing power consumption. Generally speaking, it can be applied for any

frequency crystal oscillator in electronic systems.

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