

# A 1-V 600 $\mu$ A CMOS Fractional-N Synthesizer with External Inductor QVCO for Med Radio Receiver

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**Abstract**—An ultra-low-power low voltage fractional-N synthesizer with I, Q output for 401–406 MHz Medical Device Radio communications Service (MedRadio) receiver intended for wireless communication in biomedical sensor applications is implemented using 0.18- $\mu$ m CMOS technology. The synthesizer consists of QVCO with external inductor, crystal oscillator, phase frequency detector, charge pump, prescaler and 2nd order delta sigma modulator. The fractional-N synthesizer achieves a phase noise of -106 dBc/Hz at 100 kHz offset while consuming less than 0.6 mW from a 1-V supply voltage and occupying 0.5 mm<sup>2</sup> of die area

**Index Terms**—CMOS, fractional-N synthesizer, low-voltage low-power radio.

## I. INTRODUCTION

In March 2009, the Federal Communications Commission (FCC) introduced the Medical Device Radiocommunications Service (MedRadio) [1], [3], [10] band in the range of 401–406 MHz which is a wireless communication regulation specifically dedicated for biomedical telemetry. Formerly known as the 402–405 MHz Medical Implant Communications Service (MICS) band [2] allocated by the FCC in 1999 with ten 300-kHz bandwidth channels to support implant applications, MedRadio is the superset of MICS in which additional adjacent bands called the “wing bands” at 401–402 MHz and 405–406 MHz are newly designated with twenty 100-kHz bandwidth channels to provide a total of five megahertz of contiguous spectrum and accommodate both implantable and wearable sensor devices for medical use. Due to the need for reliable, continuous, and cost-effective health monitoring in hospitals and homes in recent years [3], both implantable and wearable sensor devices in Wireless Body Area Networks (WBAN) must meet ultra-low-power consumption for prolonged battery life. Since the wireless communication part of the sensor device is

usually the most power-hungry [4], it is important to reduce both the current and the supply voltage of the transceiver to minimize the power consumption without compromising the performance.

There have been several publications on low-power RF transceivers and building blocks for wearable health monitoring sensor applications using the license-free Industrial, Scientific, and Medical (ISM) and European Short-Range Device (SRD) frequency bands at 433 MHz,

868–928 MHz, and 2.4 GHz [4]–[10]. However, the 433 MHz and 868–928 MHz bands are not recognized globally while the employment of higher frequencies has the disadvantage of increased transceiver power consumption and free-space path loss. Furthermore, since the ISM and SRD bands are utilized for many other non-medical applications, it is prone to interference issues which are critical in biomedical applications where highly reliable communication is of key importance for patient health monitoring.

In this paper, we present a complete sub-mW, low supply voltage integrated frequency synthesizer. Section II briefly addresses the implemented synthesizer architecture while Section III describes the circuit design of the building blocks in detail. Section IV describes the circuit implementation and layout. Section V presents the experimental results followed by the conclusions in Section VI.

## II. ARCHITECTURE

The synthesizer is one of the critical blocks in the above proposed receiver design. The challenge lies in the sub-mW design of the whole receiver. In this receiver design, the synthesizer with QVCO that is used as The Quadrature LO signal could be used to drive the down conversion mixer for receiver side. There are mainly three types of methods to generate quadrature signals. The 1st method is use a poly-phase filter in order to cover bandwidth and generate accurate quadrature signals, three stage filter is usually needed, which will cause substantial signal loss and need a buffer to drive the LO signal, more power will be consumed. The second method is to operate the VCO at two times the frequency and then divide-by 2. This needs a CML counter to generate quadrature signal and followed by a buffer, consuming more dc power. The third method is using a quadrature VCO. The QVCO output swing is very high due to the high  $Q$  of the inductor and this directly resonates with the gate capacitances of the mixer, thus it could directly drive the down conversion mixer, without the need for LO buffer. This is optimum for low power design as the mixer also gets the largest swing and hence higher conversion gain. In this design, we choose to use the parallel cross-coupled QVCO configuration

The proposed architecture of fractional-N synthesizer is shown in Fig. 1 which includes 5MHz crystal oscillator, quadrature VCO with external bias resistors and inductors,, PFD, charge-pump, a prescaler-8/9, a 5-bit programmable counter and a 3-bit swallow counter, 10-bit 2<sup>nd</sup> order  $\Sigma$ - $\Delta$  modulator and digital control circuit. the loop-bandwidth of

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synthesizer is set to 5 kHz. Hence, the phase-noise is mainly caused by VCO core. Which is named as a low phase-noise VCO. The synthesizer uses 5MHz signal as reference and clock to delta-Sigma modulator. The output frequency of synthesizer can be obtained using the relation:

$$f_{SYNTH} = (8 \times P + S + \frac{F}{2^{10}}) \times f_{ref} \quad (1)$$

where, P and S are the values of the programmable counter and swallow counter respectively. F is the value of 10 bits 2<sup>nd</sup>-order ΣΔ modulator's register input. 10 bits and 2<sup>nd</sup> order are design is chosen for lower power consideration. The frequency resolution thus achieved is 2.441 KHz.

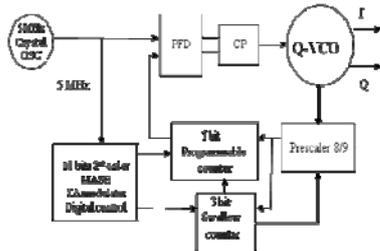


Fig. 1. Architecture of the fractional-N synthesizer.

### III. KEY BUILDING BLOCKS

#### A. Quadrature Voltage-Controlled Oscillator (QVCO)

The schematic of QVCO is shown in Fig. 2. In order to get low phase-noise and low reference spurs, the tuning sensitivity has been reduced to 35MHz/V. The phase-noise of VCO is more critical for the overall phase-noise of the synthesizer. In order to get low phase-noise, the VCO uses resistive tail current, hence, the close-in phase-noise has been improved significantly over the entire operating frequency band as the resistive tail current doesn't generate any flicker-noise. 2 high Q factor external rf inductors are used for VCO core, which could meet low phase noise and low power at same time.

#### B. Phase Frequency Detector (PFD) and Charge Pump

A dead-zone free classic phase frequency detector (PFD) is employed for phase and frequency comparison to ensure wide lock range. The current of charge-pump is set to 20uA from low power design perspective. An external loop filter is connected at the junction of charge pump output and the control voltage of the VCO.

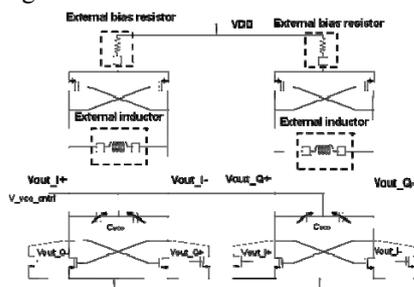


Fig. 2. Schematic diagram of QVCO.

#### C. Phase Frequency Detector (PFD) and Charge Pump

A dead-zone free classic phase frequency detector (PFD) is employed for phase and frequency comparison to ensure

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#### D. Prescaler, Counters and 3<sup>rd</sup>-Order MASH Σ-Δ Modulator

A true-single-phase clock (TSPC) prescaler 8/9 is used for the synthesizer [9]. The prescaler consists of a divide-by-4/5 synchronous counter and a divide-by-2 asynchronous counter. In combination with 5-bit programmable counter and 3-bit swallow counter, the two counters are controlled by 2<sup>nd</sup>-order 10-bit multi-stage noise-shaping (MASH) sigma-delta modulator. The 5MHz crystal oscillator reference frequency is used as the clock for the modulator.

### IV. CIRCUIT IMPLEMENTATION AND LAYOUT

The reference spur is mainly due to the substrate and power supply reference noise coupling. The reference noise is generated from the digital circuit of synthesizer, which includes the reference counter, PFD, dividers, MASH Σ-Δ modulator. In order to reduce the noise coupling from the substrate, the analog and digital circuit are separated wide apart. QVCO include the totally balance and symmetrical layout in order to increase receiver's image rejection ration. a guard ring is added for VCO core circuit separately. Guard-ring is added to each digital circuit in order to reduce the suppress coupling of reference spur noise to synthesizer output. The spur noise from the power supply was suppressed by separating the power supplies of digital and analog circuits.

### V. MEASUREMENT

The fractional-N Synthesizer with external inductor QVCO is implemented in standard 1P6M 0.18-μm RF CMOS process with 2-μm top metal and MIM capacitor options.

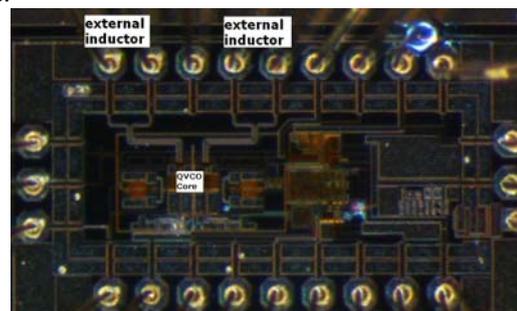


Fig. 3. Chip microphotograph (die size: 1.0.mm x 0.5mm).

The microphotograph of the test chip is shown in Fig.3. QVCO core have good match and symmetrical layout. The die area including the pads occupied is 1.0mm × 0.5mm. The test chip was packaged in a commercial QFN package and evaluated with external inductors on a low-cost FR4 board is shown in Fig.4.

In Fig.5. the measured phase-noise plot at 401MHz is shown with the loop filter bandwidth of 5 kHz. The phase-noise at 100 kHz offset is -106dBc/Hz, 1MHz offset is

-130dBc/Hz, the measurement summary is shown in Table I. the current consumption of synthesizer block is shown in Table II.

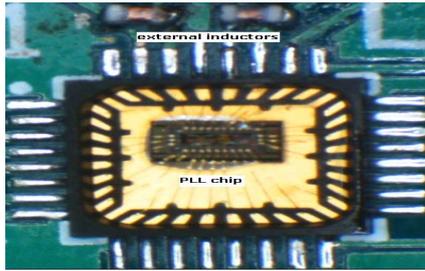


Fig. 4. The chip QFN package with 2 external inductor on FR4 PCB board.

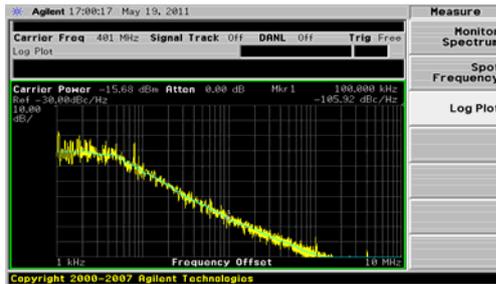


Fig. 5. Measured phase-noise.

TABLE I: MEASUREMENT SUMMARY OF FRACTIONAL-N SYNTHESIZER

Parameter	Measurement
power supply	1V
Frequency range	395-415 MHz
Frequency Deviation ( $\Delta f$ )	2.441 KHz
Phase Noise	-106 dBc/Hz @ 100 KHz
Phase Noise	-130 dBc/Hz @ 1 MHz
Spur	-55 dBC
Power (PLL/with IQ out)	600uA@1V

TABLE II: CURRENT CONSUMPTION OF SYNTHESIZER BLOCKS

Block	mA
QVCO+buffer	0.37
5M crystal OSC	0.05
Prescaler8/9	0.1
PFD & CP	0.08
Total	0.6

## VI. CONCLUSION

Design, implementation and measurement results of medradio fraction-N synthesizer have been presented. The chip consumes 600uA from a single 1V power supply achieving -106dBc/HZ at 100KHz offset. Since the synthesizer is fully integrated onto the chip, makes it to convenient to integrate with other low power transceiver blocks achieving excellent performance of the overall transceiver.

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