# A 52nW, 18ppm/°C, Voltage Reference Circuit using BJTs and Subthreshold Mosfet

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***Abstract*—A voltage reference circuit which utilizes a pair of BJTs and a MOSFET operating in subthreshold mode is designed in 0.13um CMOS 1P6M process. The proportional to temperature (PTAT) signal is derived using a pair of BJTs, while complementary to temperature (CTAT) signal is realized as gate to source voltage of subthreshold MOSFET. It requires smaller silicon area and is less sensitive to mismatches compared to the conventional bandgap generation circuit. The reference circuit works well from 1.3V to 3.6V. It has temperature stability 18ppm/°C for reference voltage of 1.0V in the temperature range of -40°C to 85°C and it consumes 52nW power.**

***Index Terms*—Voltage reference, low power bandgap voltage circuit, CTAT, PTAT, nano power, subthreshold MOSFET**

## I. Introduction

The battery-operated CMOS based electronic devices market is growing every year. To increase battery life, it is required to design circuit building blocks with lower supply voltage and consuming sub-microwatt power. Among them voltage reference circuits are essential in any CMOS design. They are used in almost all analog and digital systems to generate a DC voltage independent of the supply voltage and of temperature variations [1]. Some of the systems on chip (SoC's) have special modes called sleep or standby modes, in which only a small part of the SoC is functional and the main part is switched off. It is quite possible that the SoC may spend long durations in these modes. To save the battery life, the SoC's should consume as low power as possible. They are normally required to consume power is sub-microwatts. Reference circuits are usually required to operate under these modes. Our target is to meet the power consumption for the reference circuits in nano-watts.

Reference voltage is made independent of supply voltage by designing appropriate circuit architecture. Reference voltage is made temperature independent by using the weighted summation of a Proportional to Absolute Temperature (PTAT) signal and a Complementary to Absolute Temperature (CTAT) signal. With convenient weights, the negative and positive variations of the signals will cancel each other and a temperature stable voltage can be reached. The most common solution is the use of a bandgap voltage reference circuit, which can be implemented in any standard CMOS technology by exploiting the parasitic vertical BJTs [2], [3].

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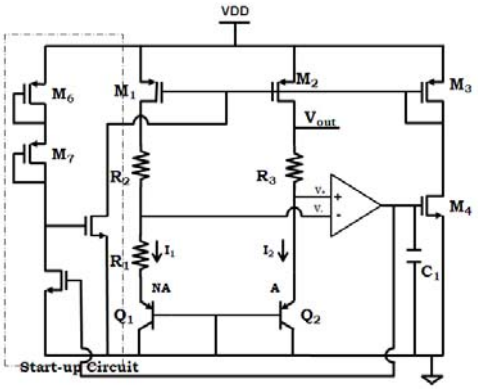


Fig.1. Conventional bandgap circuit schematic

The conventional bandgap circuit employing the BJTs is shown in Fig. 1. In this topology, PTAT signal is generated by the difference of base-emitter voltages ($V_{BE}$) of the BJTs $Q_1$ and $Q_2$.

The opamp in the circuit of Fig. 1 maintains equal voltages at its input ports (shown as $V_+$ and $V_-$ in Fig. 1 schematic). Hence, the following equation holds:

$$V_+ = V_- = V_{BE\,Q2} = V_{BE\,Q1} + I_1 R_1 \tag{1}$$

where, $I_1$ is the emitter current in transistor $Q_1$. Sizes of the MOSFET's *$M_1$, $M_2$, and M3* are equal. If current in the emitter of $Q_2$ is $I_2$ then analyzing the topology of the circuit it can be written as:

$$I_1 = I_2 \tag{2}$$

If the ratios of the emitter areas of $Q_1$ and $Q_2$ is $N$, relation between the collector current densities $J_1$ and $J_2$ is as follows:

$$J_1 = J_2 / N \tag{3}$$

Using the basic operational equation of BJTs, following relation between $N$ and $V_{BE}$'s of BJTs can be derived:

$$\Delta V_{BE} = V_{BE\,Q2} - V_{BE\,Q1} = \frac{kT}{q} \ln N \tag{4}$$

Plugging (4) into (1), the current in the resistor $R_1$ is given by the following equation:

$$I_1 = \frac{kT}{qR_1} \ln N \tag{5}$$

It is evident from (5) that the current $I_1$ and hence the

voltage across the resistor $R_1$ are PTAT signals, which are used in the circuit of Fig. 1 to derive the reference voltage. The base-emitter voltage ($V_{BE}$) of the BJT has negative temperature coefficient for a constant current [4] and it is used as the CTAT signal directly for deriving bandgap voltage in the circuit of Fig. 1. If the negative temperature coefficient of $V_{BE}$ is $K_1$, we can write the following equation:

$$\left(\frac{\partial V_{BE}}{\partial T}\right)_{T_O} = -K_1 \tag{6}$$

The output of reference generation circuit can be written as sum of base-emitter voltage of $Q_2$ and voltage drop across resistor $R_3$:

$$V_{out} = V_{BEQ2} + \frac{kT}{q}\left(\frac{R_3}{R_1}\right)\ln N \tag{7}$$

($\partial V_{out}/\partial T$) is equated to zero for cancelling the temperature coefficient:

$$\left(\frac{\partial V_{out}}{\partial T}\right)_{T_O} = 0 = -K_1 + \frac{k}{q}\left(\frac{R_3}{R_1}\right)\ln N \tag{8}$$

From (8), it is quite obvious that choosing an appropriate ratio for $R_3$ and $R_1$ results in cancelling the temperature coefficient of the output voltage.

## II. The Proposed Nano Power Voltage Reference Circuit And Its Analysis

In order to achieve power consumption in nano watts using the conventional bandgap reference, described in section I, requires large resistors in the range of several mega ohms. Large resistors result in occupying a larger portion of the silicon area. Also, accuracy of the bandgap voltage generation in conventional bandgap generation circuit is determined by the matching accuracy between the resistors $R_1$, $R_2$ and $R_3$. Matching requirement between the resistors makes the layout design of the bandgap circuit more challenging.

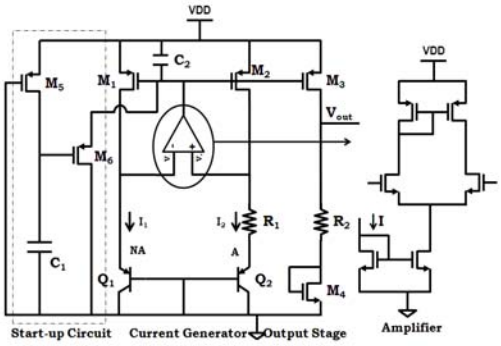


Fig. 2. The proposed voltage reference circuit schematic

The proposed circuit is shown in Fig. 2. To handle the above mentioned problems, we exploit the CTAT characteristics of the threshold voltage of the subthreshold MOSFETs [5]. The PTAT signal is realized by the current generated by the BJT pair, while the CTAT signal is realized by the $V_{GS}$ of MOSFET $M_4$ operating in the subthreshold mode. Both the signals are added to cancel the temperature coefficient

The PTAT signal in the proposed circuit is derived based on the same principles as in the conventional circuit of Fig. 1. Using the similar analysis, current $I_1$ can be determined as follows:

$$I_1 = \frac{kT}{qR_1}\ln N \tag{9}$$

$I_1$ is the current in the resistor $R_1$. This current is mirrored from MOSFET $M_2$ to $M_3$ and supplied to the MOSFET $M_4$. Sizes of MOSFETs $M_1$, $M_2$ and $M_3$ are equal. The voltage across the resistor $R_2$ ($V_{R2}$) is a PTAT signal and can be written as follows:

$$V_{R_2} = \frac{kT}{q}\left(\frac{R_2}{R_1}\right)\ln N \tag{10}$$

The characteristic of a MOSFET operating in sub-threshold region is similar to a bipolar transistor in which the drain current varies exponentially with the gate-source voltage. The characteristic of a MOSFET operating in sub-threshold region is given by [6]:

$$I_{ds} = \mu C_{ox}\left(\frac{W}{L}\right)V_T^{\,2} e^{\left(\frac{V_{GS}-V_{TH}}{nV_{TH}}\right)}\left[1-e^{\left(-q\frac{V_{DS}}{nT}\right)}\right] \tag{11}$$

where $n$, $\mu$, $W/L$, $V_T$, $V_{DS}$, $V_{GS}$, $V_{TH}$, $C_{ox}$ and $T$ represents the slope factor, mobility, thermal voltage, drain-source voltage, gate-source voltage, threshold voltage, gate-oxide capacitor and temperature respectively.

The mobility $\mu(T)$ is a function of temperature and described by (12):

$$\mu(T) = \mu(T_0)(T/T_0)^{-m} \tag{12}$$

where $\mu(T_0)$ is the mobility at the reference temperature and$1 \leq m \leq 2$. [6]

If $V_{DS} >> V_T$ (which is satisfied for the diode connected MOSFET $M_4$) the last term in (11) can be neglected. Substituting (12) in (11), the gate-source voltage can be derived from (11) as:

$$V_{GS} = V_{TH} + nV_T \ln\left[\frac{I_{ds}L}{n\mu(T_0)(T/T_0)^{-m}C_{ox}WV_T^{\,2}}\right] \tag{13}$$

Assuming that the current is constant and $m$=2, then differentiating the gate to source voltage with respect to temperature yields:

$$\frac{\partial V_{GS}}{\partial T}=\frac{\partial V_{TH}}{\partial T}+\frac{nK}{q}\ln\left[\frac{I_{ds}LT_O^{\,2}}{n\mu(T_o)C_{ox}WV_T^{\,2}}\right] \quad (14)$$

The term within the ln operator is smaller than 1 and thus the second term is negative. The temperature coefficient of the threshold voltage is also negative leading to a overall negative temperature coefficient for the gate-source voltage. If the total negative temperature coefficient of $V_{GS}$ is $K_2$, (14) can be simplified as follows:

$$\left(\frac{\partial V_{GS}}{\partial T}\right)_{T_O}=-K_2 \quad (15)$$

$V_{GS}$ is used as CTAT signal for generating reference voltage in the proposed circuit. The output voltage can be written as sum of gate source voltage of MOSFET $M_4$ and the voltage drop across resistor $R_2$:

$$V_{out}=V_{GS\,M4}+\frac{kT}{q}\left(\frac{R_2}{R_1}\right)\ln N \quad (16)$$

Equating ($\partial V_{out}/\partial T$) to zero results in the desired equation (17) for cancellation of temperature coefficient of output voltage.

$$\left(\frac{\partial V_{out}}{\partial T}\right)_{T_O}=0=-K_2+\frac{k}{q}\left(\frac{R_2}{R_1}\right)\ln N \quad (17)$$

From (17), it is clear that choosing an appropriate ratio of $R_2$ and $R_1$ results in cancelling the temperature coefficient of the output voltage.

## III. Design Procedure and Simulation Results

### A. Minimum Supply Voltage

Minimum power supply voltage (*VDD*) for the proposed circuit is decided by the value of reference voltage and by the condition that the drain to source voltage drops for MOSFETs $M_1$, $M_2$ and $M_3$ should be more than few times of thermal voltage ($V_T$). The later condition is required so that the exponential term containing $V_{DS}$ in (11) can be neglected.

$$VDD > V_{ref}+10V_T \quad (18)$$

The value of the reference voltage is obtained around 1.0 V and $V_T$ is around 26mV. Hence minimum supply voltage that can be used is 1.26V.

### B. Design for Minimum Power Consumption

In this design the limiting factor on the power consumption only comes from the leakage currents. The leakage current increases as the temperature increases [7]. The leakage current can be 100pA at 100 degree C, 1nA at 125 degree C [7]. To minimize error in the reference generation, the current in the transistors is kept 10nA.

### C. Design Values Used in the Circuit

The value of PTAT current at room temperature is determined by the ratio of areas of $Q_1$ and $Q_2$ and value of the resistor $R_1$. The area ratio is kept *8*. To make the PTAT current equal to 10nA, the value of resistor $R_1$ is determined bases on (9) and its value in our design is 6.1Meg Ohms. Value of the resistor $R_2$ is chosen as to cancel the temperature coefficient and decided from (18). The value of the resistor $R_2$ is 33.5Meg Ohms in our design.

Fig. 4 shows the variation of reference voltage with respect to temperature for different resistance ratios. It can be seen that a particular resistance ratio optimizes the temperature stability.

Temperature stability curve for the proposed voltage reference is shown in Fig. 3 and it is 18ppm/°C.

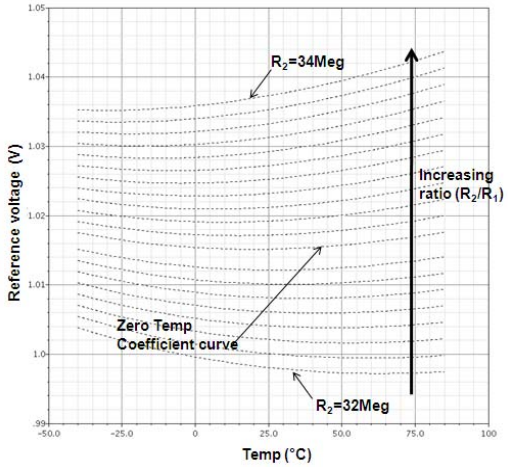


Fig. 3. Reference voltage variation with the temperature for various resistance ratios in proposed reference generation circuit

The circuit is simulated for different power supply voltage. *VDD* is varied from *1.3V* to *3.6V*. Fig. 5 shows temperature stability curves for different *VDD*s. It can be seen that zero temp coefficient remains around 25°C for all *VDD*s and the reference voltage variation with temperature is approximately same for all the curves.

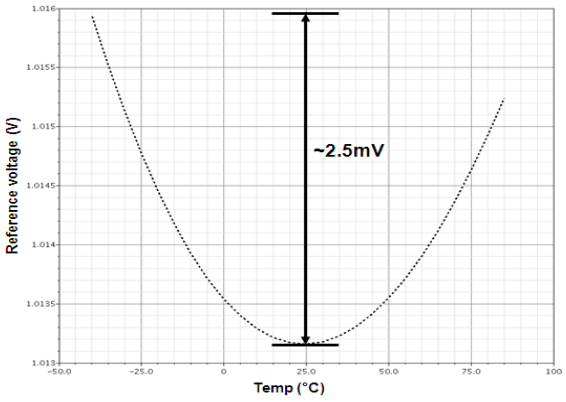


Fig. 4. Temperature stability curves of the proposed voltage reference circuit.

### D. Layout of the Proposed Voltage Reference Circuit

The layout of the proposed circuit is shown in Fig. 6. It occupies 0.16x0.18mm$^2$ of silicon area. The BJT pair, resistors $R_1$ and $R_2$, and stability capacitance $C_2$ in the

proposed circuit in Fig. 2 are shown in the layout. The resistors $R_1$ and $R_2$ are matched inter-digitally in the layout to increase reference voltage generation accuracy. They occupy 60% area of the full circuit layout. As the proposed circuit requires one less resistor of large value, it has merit for the silicon area and matching sensitive performance compared to the conventional bandgap voltage reference circuit.

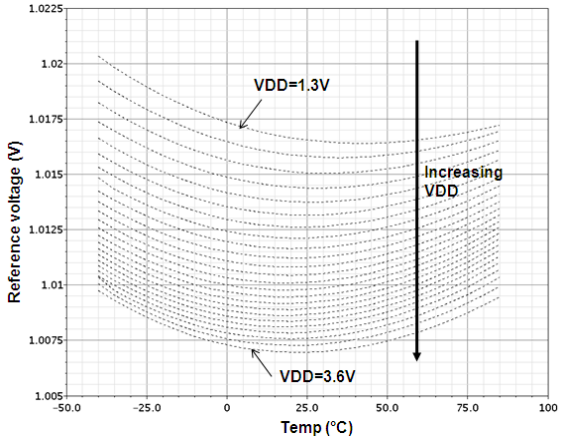


Fig. 5. Temperature stability curves of the proposed voltage reference circuit for different power supply voltage.

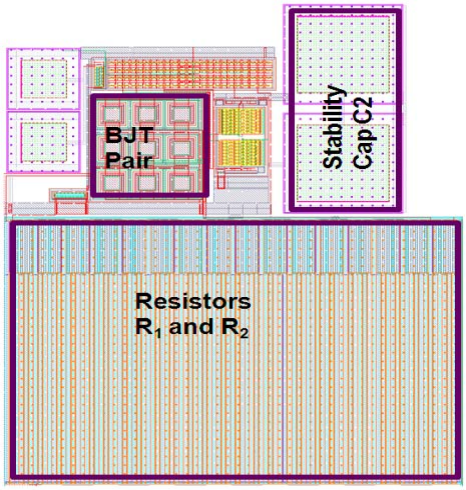


Fig. 6. Layout of the proposed voltage reference circuit

## IV. Conclusion

A nano power reference voltage is designed and it utilizes BJTs and a MOSFET operating in subthreshold region to cancel the temperature coefficient of the reference voltage. Using the subthreshold MOSFET in the proposed circuit, requires one less resistor of large value of several mega ohms than the conventional bandgap circuit and also it reduces the matching requirement for the layout of the circuit. The proposed circuit consumes 52nW and the supply voltage is 1.3V. The temperature stability is 18ppm/°C. It is designed in 0.13um CMOS 1P6M process.

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