Dual Channel High Precision 26 Bit Frequency Counter Using CPLD XC95108XL for QCM Sensor System

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***Abstract*—Frequency counter is main part of the instrumentation system for QCM sensor. Precision and stability of the frequency counter together with the compactness of the frequency counter are crucial factors in development of frequency counter for QCM sensor. CPLD is one of the good choice to be used as a core device to develop frequency counter. The design of the CPLD to be used as a frequency counter can be easily implemented as the availability of CPLD big amount of macrocells is existed. However, careful system design is also needed to optimize the used of the CPLD resources. In the development of CPLD as frequency counter, data transfer from CPLD to microcontroller plays a significant role to the resource usage. In the use of Xilinx XC95108 as 26 bit dual frequency counter, data transfer with 4 bit data width is the most appropriate one to be implemented. The developed frequency counter shows a high accuracy, precision and stability. The developed frequency counter has a 1 Hz precision and stability.**

***Index Terms*—QCM sensor, frequency counter, CPLD.**

I. Introduction

Quartz Crystal Microbalance (QCM) is one of the mass sensitive sensors, which is used widely for biosensor. There is an increasing number of application has been reported on the development of QCM biosensor. Many different working principles are used based on the QCM behavior as sensing device. Every working principle in used is then followed by the development of an appropriate instrumentation system which has a different electronic circuit such as reposted in many papers [1]-[3].

The first principle work of the QCM sensor is based on frequency change as described by Sauerbrey in 1957. Other techniques such as impedance change or dissipating signal detection has been used. The used of QCM sensor based on the frequency change is one of the simplest methods and widely used even in a QCM array sensor [4], liquid application [5], [6] or gas sensor [7], [8]. In this approach, the sensitivity of the sensor depends on the fundamental frequency of the sensor and also resolution and stability of frequency counter. To achieve high sensitivity, the frequency counter must be able to distinguish a change of the QCM frequency down to 1 Hz resolution in every second or even better. In addition, the frequency counter must have a counting stability down to 1 Hz over the measurement period. Better frequency change detection will also improve the sensitivity of the sensing system, but also needs careful design of the overall system. In many cases, 1 Hz resolution of the frequency counter in used is adequate.

High-precision frequency counter can be developed by using discrete electronic device, microcontroller, CPLD, FPGA and other microelectronic devices. Development of frequency counter becomes easier and more efficient by using FPGA; CPLD and microcontroller compare to the discrete electronic device Microcontroller providing excellence ability and simplicity for simple computational work. Moreover, the availability of communication modules makes the microcontroller can be directly connected to other devices, including computer through serial communication. By using a single-chip microcontroller, one can build a limited, usually single channel frequency counter, by utilizing internal timer and counter of the microcontroller. However, adjustment to get high accuracy and precision of counting, which is mainly based on the accuracy and precision of the timer is not as good as the discrete logic device.

The advance of microelectronic technology provides many types of a programmable device such as FPGA and CPLD. FPGA which consists of a very high density logic circuit which can be programmed can be configured for multichannel frequency counter. In other hands, CPLD has a faster pin to pin signal. Baronti et all [9] shows how an FPGA together with DSP can be used as a core for multi-channel configurable counter. The use of FPGA as a basis for frequency counter also discussed in some papers [3]. Frequency counter using lower density logic circuit in form of ASIC has also been presented [10] with good accuracy and precision.

Building such of counter in CPLD or FPGA is not a difficult task as we can select a CPLD or FPGA, which can fill the requirement, by selecting a big resources devices. However, in some situation if the system is not well designed the resources' utilization will become inefficient. This paper shows how a simple problem in the data bus width transfer between devices affects the utilization of the resources. We developed a dual-channel frequency counter using CPLD Xilinx XC95C108XL, XC9536XL and PIC18F4550 Microcontroller. We have utilized the maximum available XC95108XL macrocells and logic block to construct 26bit frequency counter. By combining the data communication and control from both CPLD and the microcontroller, high-precision frequency counter up to 26bit with a resolution of 1 Hz can be realized. This system is adequate to be used for a QCM sensor application to measure the resonance frequency up to 65MHz. This range is good enough to be used as for liquid environment application many QCM sensors work in a frequency less than 20 MHz.

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II. System Design

Conventional frequency counter is basically constructed by a time gate and digital counter as in Fig. 1. For QCM sensor application, a one-second acquisition rate is needed to be used in many applications. Thus, we can directly get the sensor frequency from the digital counter without any further processing. In this design, we used a microcontroller (PIC18F4550) to collect and processed the signal from oscillator to be send to a host computer.

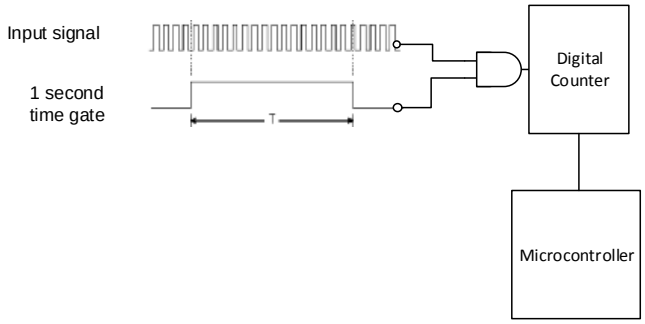

Fig. 1. Frequency counter block system.

Core of the frequency counter is the one-second timer and the digital counter. The one-second timer can be implemented by using many difference systems. In this design, we use CPLD XC9536XL together with a 20MHz clock source by using TCXO with accuracy and precision of 0.3ppm. A 25 bit digital counter is implemented inside the XC9536XL in order to divide the 20MHz clock source to generate a 1 Hz signal. The one second high state signal is generated by the CPLD by counting the incoming clock pulse in amount of 20 million pulse. Thus theoretically, the highest accuracy of the one-second timer is 50nS.

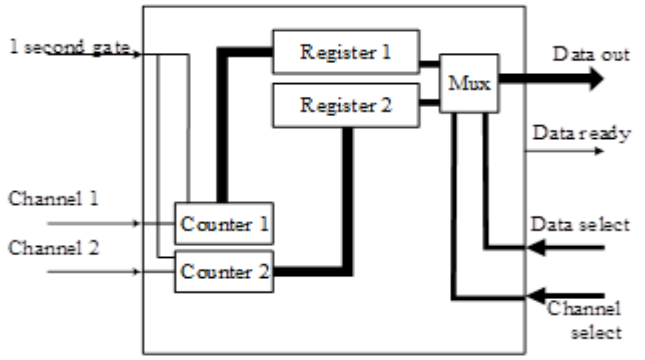

Fig. 2. Block diagram of the implemented dual channel 26bit counter.

Digital counter in the design is simply implemented in VHDL by a mechanism of increasing content of a register which is implemented as a dynamic variable. In this implementation, we built based on a generic algorithm and let the compiler do the optimization. The block diagram of the digital counter system to be implemented is presented in Fig. 2.

Based on the schematic diagram in Fig. 3, an algorithm to make the system work is listed in Fig. 3.

The implementation of counter is simply by increasing the value of an internal register which is control by 1 second gate signal (high) and signal input.

1. Start
2. If rising edge detected in gate signal set data ready to 1
3. If gate signal=1 do
   a. Count channel 1 and channel 2
   b. Transfer data from register to Data Out based on data select and channel select
4. If falling edge detected in gate signal do:
   a. Stop counting
   b. Copy data in Counter 1 to Register 1
   c. Copy data in Counter 2 to Register 2
   d. Reset Counter 1 to 0
   e. Reset Counter 2 to 0
5. Go to 2
6. End

Fig. 3. Algorithm of the digital counter system.

```
Process(Channel1, gate_signal, counter1)
begin
   if gate_signal = '0' then Counter1 <= 0;
      elsif (Channel1'event and Channel1='1') then
         Counter1 <= Counter1 + 1;
   end if;
end Process;

Process(Channel2, gate_signal, counter2)
begin
   if gate_signal = '0' then Counter2 <= 0;
      elsif (Channel2'event and Channel2='1') then
         Counter2 <= Counter2 + 1;
   end if;
end Process;
```

Fig. 4. Up counter implementation.

Data transfer from the internal register of the counter to the output register is done as in Fig. 5. The data transfer is done as the one-second gate signal change it states from 1 to 0. In this transition (1 to 0) the data ready signal is set to 0. Condition zero of the one-second gate is maintained for 50nS (1 pulse of 20MHz) to allow the data transfer from the counter to the internal register in the CPLD done completely. As the one-second gate signal changes it states from 0 to 1 the data ready signal is set to 1. The data ready signal is sent to the interrupt of the microcontroller to read the data in the register, processed and send to the PC. Data-transfer process is fully controlled by the microcontroller to shift data from the register in the CPLD to the register of the microcontroller.

```
Process(gate_signal)
begin
if gate_signal'event and gate_signal = '0' then
                register1 <= counter1;
                register2 <= counter2;
end if;
end Process;
```

Fig. 5. Data transfer from internal register counter to output register.

Data transfer from the register to the microcontroller is done by sending the data through a bus to the digital I/O of the microcontroller. Based on the availability of the digital I/O port of the microcontroller in used, the bus width can be varied from 1 bit to 24 bit data (maximum available digital I/O port of the microcontroller). Implementation of the algorithm in Fig. 3 in a CPLD is an easy task. It will be

effortless to implement the algorithm in a CPLD which has large macrocells such as Xilinx XC2C256, XC95288 or bigger capacity one. However, in this experiment we found that careful design needs to be made to implement the algorithm in XC95108XLwhich only has 108 macrocells.

The algorithm of the CPLD task in Fig. 3 can be divided by three main tasks, which is done sequentially. First task is counting process; data transfer to the register and finally data transfer to the microcontroller. The sequence of this process is also reflected in the resource usage. The flow of the tasks is controlled by 1 second gate signal; data select and channel select. The used of the internal register is to make the counter to work without affected by data transfer to the microcontroller. The multiplexer is used to transfer the 26 bit data out to fit with digital I/O of the microcontroller. To be mention here that not all 24 bit digital I/O port of the microcontroller (PIC18F4550) can be used as some of the digital I/O channel used for other purposes (data communication to PC, interrupt and others).

III. Experimental Result and Discussion

A. Fitting and Simulation

In this design, we have design a two channel 26 bit counter in the CPLD. During the design, we found that the combination of counter length and bus width for the data transfer plays an importance role in the fitting process. Bus width and register specifically affect the use of macrocells of the Xilinx CPLD. Longer register required more logic blocks. As the data transfer through the bus also requires memory, this also affects the fitting process. As the length of the counter must be 26 bits to hold an input signal up to 50MHz, optimization is done by changing the bus width.

Data bus with 8 bit width is a most comfortable choice to transfer the data to the microcontroller and result in a simple algorithm in the microcontroller to construct back into 26bit data. However, designing an 8 bit data bus width cannot be fitted in the Xilinx XC95108XL. Eight-bit data bus requires 102 macrocells to be implemented, whilst the CPLD only has 108 macrocells. Changing the data bus width into 4 bits results in a good fit process. The system reports the usage resource for 108 macrocells, 104 register and 194 function block. Decreasing the bus width into 2 bit data make the system use 110 macrocells which cannot be fitted to the XC95108XL.

Table I shows a summary of the fitting result as we varied the bus width of the data transfer to microcontroller. The variation of the bus width is made in a form of 2n line to make a simple data processing in the microcontroller. In Table I, we can see that only system with 4 bit data output bus can be fitted to the CPLD whilst the others cannot be fitted as it requires macrocells more than 108 macrocells.

TABLE I: Bus Width of Data Output and Macrocells Used in XC95108

Bus width	Macrocells	Fitting
1	121	Fail
2	110	Fail
4	108	Success
8	112	Fail
16	120	Fail
26	130	Fail

Based on the same schematic design and algorithm, investigation to check resource usage by the CPLD was tested by implementing the algorithm in a bigger CPLD which has similar technology. In our simulation we tested on XC95288 which has 288 macrocells. The relationship between bus width and resource usage presented in Table II. We can see that all bus width can be fitted into the CPLD. It can be seen that the 4 bits bus width consumes minimum macrocells compare to the other system with other data bus widths.

Timing diagram from the simulation process for the 4 bit data bus width is presented in Fig. 6. In this simulation result, we can see that the system works well. The value of the counter increase during the high condition of timer gate signal. At falling transition of the timer gate signal (at 999.999.950ns) the counter is reset to zero and the output register holds the counted signal. Data output to the microcontroller is done after high transition of the timer gate signal (at 1.000.000.050ns). This cycle is repeated every second.

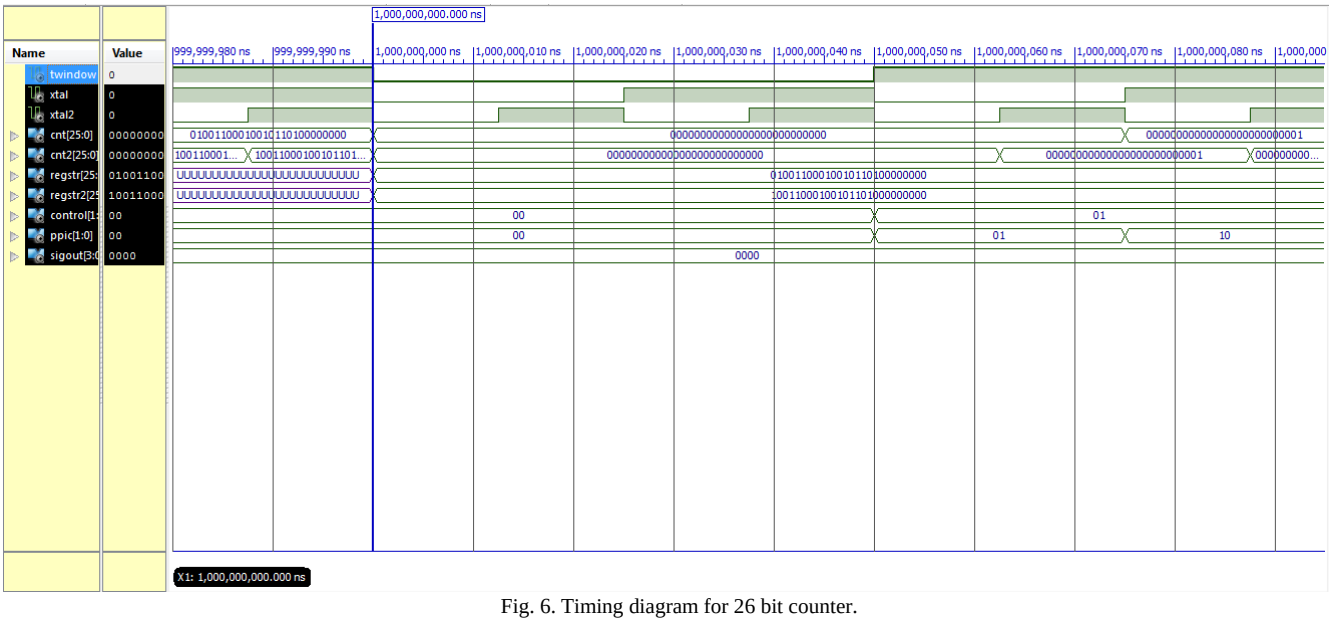

Fig. 6. Timing diagram for 26 bit counter.

TABLE II: BUS WIDTH OF DATA OUTPUT AND RESOURCE USED IN XC95288

Bus width	Macrocells	P-term	Register	Function block input	Note
1	121	328	104	228	Success
2	110	315	104	188	Success
4	**108**	**310**	**104**	**201**	**Success**
8	112	310	104	199	Success
16	120	310	104	252	Success
26	130	310	104	245	Success

A. Board Implementation and Measurement Result

The system is implemented on a PCB board as presented in Fig. 7. To achieve a good accuracy the one-second time gate signal which is generated from 20MHz TCXO was tuned to a standard rubidium frequency source. Standard frequency 10.000.000 Hz rubidium oscillator with long-term stability < 2×10-11/day (SpectraTime LCR-900) was used to calibrate the time gate.

Fig. 7. System board.

Fig. 8 shows the frequency of the rubidium oscillator after time signal adjustment and some TCXO oscillator sources. From Figure 8, we can see that the recorded output frequency from 10Mhz Rubidium oscillator is changing from 10.000.000Hz and 10.000.001Hz. The precision of the frequency counter is 1 Hz. This 1 Hz precision is due to the signal level transition which cannot be predicted its occurrence and cannot be synchronized with the 1 second gate signal transition. Improvement of the precision can be done by using dual edge counter but it will consume more resources which cannot be fitted to the devices. For better resolution by using dual edge or reciprocal counter, more resource needed and possibly can be implemented using bigger capacity CPLD.

From the resulting frequency measurement in Figure 8, we can see that this frequency counter is stabile for long time measurement, which is suitable for common frequency measurement for QCM sensor. The frequency counter also able to count output signal from TCXO with a precision and stability of 1 Hz.

IV. CONCLUSION

Simple and low cost frequency counter with high accuracy and precision for QCM sensor can be implemented using CPLD and microcontroller. High precision and stability of the counter can be achieved by using a good TCXO as a basis for one-second timer. In the design of the CPLD with microcontroller as a frequency counter, the data bus width to transfer the value of the digital counter in CPLD to microcontroller needs to be optimize to fit into the CPLD. Using Xilinx XC95108 and XC95288 a data bus width of 4 bits is the optimal condition to be implemented in the CPLD to transfer the data to the microcontroller.

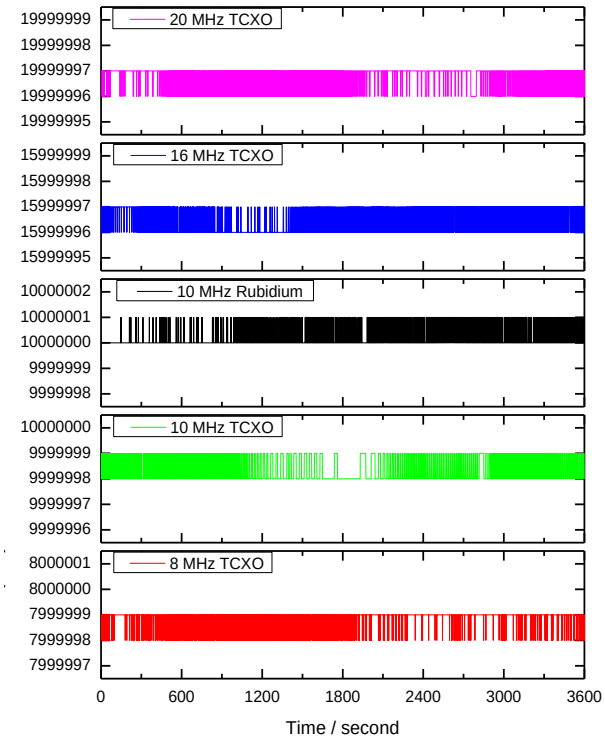

Fig. 8. Recorded frequency from several TCXO and 10MHz Rubidium oscillator.

REFERENCES

[1] A. Arnau, "A Review of interface electronic systems for at-cut quartz crystal microbalance applications in liquids," *Sensors*, vol. 8, no. 1, pp. 370–411, Jan. 2008.

[2] J. Schroeder, R. Borngraeber, F. Eichelbaum, and P. Hauptmann, "Advanced interface electronics and methods for QCM," *Sensors and Actuators A*, vol. 98, pp. 543–547, 2002.

[3] J. Auge, K. Dierks, F. Eichelbaum, and P. Hauptmann, "High-speed multi-parameter data acquisition and web-based remote access to resonant sensors and sensor arrays," *Sensors and Actuators B*, vol. 95, pp. 32–38, 2003.

[4] A. Tuantranont, A. Wisitsora-at, P. Sritongkham, and K. Jaruwongrungsee, "A review of monolithic multichannel quartz crystal microbalance: a review," *Analytica Chimica Acta*, vol. 687, no. 2, pp. 114–28, Feb. 2011.

[5] S. P. Sakti, F. Wahyuni, U. P. Juswono, and Aulanni'am, "Development of qcm immunosensor with small sample solution for detection of mmp-3 antibody," *Sensors and Transducers*, vol. 149, no. 2, pp. 143–148, 2013.

[6] F. Liu, Y. Li, X. L. Su, M. F. Slavik, Y. Ying, and J. Wang, "QCM immunosensor with nanoparticle amplification for detection of Escherichia coli O157:H7," *Sensing and Instrumentation for Food Quality and Safety*, vol. 1, no. 4, pp. 161–168, Sep. 2007.

[7] L. R. Khot, S. Panigrahi, and D. Lin, "Development and evaluation of piezoelectric-polymer thin film sensors for low concentration detection of volatile organic compounds related to food safety applications," *Sensors & Actuators: B. Chemical*, vol. 153, no. 1, pp. 1–10, 2011.

[8] R. Selyanchyn, S. Korposh, S. Wakamatsu, and S. W. Lee, "Respiratory monitoring by porphyrin modified quartz crystal microbalance sensors," *Sensors*, vol. 11, no. 1, pp. 1177–91, Jan. 2011.

[9] F. Baronti, A. Lazzeri, R. Roncella, and R. Saletti, "FPGA / DSP-based implementation of a high-performance multi-channel counter," *Journal of Systems Architecture*, vol. 55, no. 5–6, pp. 310–316, 2009.

[10] J. M. Beeley, C. Mills, P. A. Hammond, A. Glidle, J. M. Cooper, L. Wang, and D. R. S. Cumming, "All-digital interface ASIC for a QCM-based electronic nose," *Sensors and Actuators B: Chemical*, vol. 103, no. 1–2, pp. 31–36, Sep. 2004.

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