DVCC-Based First-Order Filter with Grounded Capacitor

Hua-Pin Chen, Kuo-Wei Huang, and Po-Ming Huang

***Abstract*—A new first-order voltage-mode filter employing minimum active and passive components is proposed. The proposed configuration employs one differential voltage current conveyor (DVCC), one grounded capacitor and one resistor. It maintains the following advantageous: (i) employment of only one current conveyor, (ii) employment of only one grounded capacitor, (iii) employment of only one resistor, (iv) simultaneous realization of voltage-mode first-order lowpass, highpass and allpass filter responses from the same configuration, (v) no need to impose component choice conditions and (vi) low active and passive sensitivity performances. HSPICE simulation results using TSMC 0.18μm 1P6M CMOS process technology and ±0.9V supply voltages validate the theoretical predictions.**

***Index Terms*—Active filters, voltage-mode; DVCC, first-order filter.**

I. INTRODUCTION

At present there is a growing interest in designing analogue current-mode signal-processing circuits. In these circuits the current rather than the voltage is used as the active variable either throughout the whole circuit or only in certain critical areas [1]. The use of current-mode active devices has many other advantages such as larger dynamic, higher bandwidth, greater linearity, simple circuitry and low power consumption compared to that of voltage-mode counterparts for example operational amplifiers [1]. Filters are widely used in many communications, signal processing, automatic control, and instrumentation systems. For examples, two system block diagrams of the receiver/transmitter part of a global system for mobiles (GSM) cellular telephone and crossover network used in a three-way high-fidelity loudspeaker are introduced in [2, 3]. As a current-mode active device, the differential voltage current conveyor (DVCC) has the advantages of both of the second generation current conveyor (such as large signal bandwidth, great linearity, wide dynamic range) and the differential difference input amplifier (such as high input impedance and arithmetic operation capability) [4]. This element is a versatile building block whose applications exist in the literature [4–10]. Allpass filters can offer a reliable and telling method to change the phase of an electronic signal without affecting the amplitude over the frequency in controlling and communicating applications. Obviously, allpass filters just has the above the important performance which can not be replaced by any others filters. Therefore, many first and high order allpass filters have been researched and reported since 1966 [11–20]. Recently, first-order allpass filters using only single current conveyor with less passive elements have been published in [16–19]. However, these configurations required at least two resistors and one capacitor, which were not minimum components to realize the first-order filters, and these configurations also needed one matching condition to realize the allpass filters. Although, the first-order allpass filters using only a single current conveyor with minimum passive components (one resistor and one capacitor) had been published in [20], it still needs a component choice condition to realize allpass filter response. Moreover, the capacitor was floating in the above proposed configuration. Obviously, no allpass filter circuits [16–20] have been reported to date which simultaneously achieve all of the advantageous features as follows: (i) employment of only one current conveyor, (ii) employment of only one grounded capacitor, (iii) employment of only one resistor, (iv) no need to impose component choice conditions, and (v) low active and passive sensitivities. In this paper, the authors proposed a simple first-order filter employ minimum active and passive components. The proposed circuit can realize first-order lowpass, highpass and allpass filter responses in the same configuration and still enjoys all of the above features. Meanwhile, a filter having only grounded capacitors is convenient for integrated circuit (IC) implementation. It is well known that floating capacitors can be realized if the IC process offers double poly layers. Recently, a floating capacitor can also be realized as Metal-Insulator-Metal (MIM) capacitor. The dominant parasitic capacitance of a double-poly integrated capacitor which is between bottom plate and ground can be suppressed in MIN capacitors. However, grounded capacitors can absorb parasitic capacitances and may have less parasitics compared to floating counterparts. The use of only a grounded capacitor is suitable for integrated circuit implementation [21].

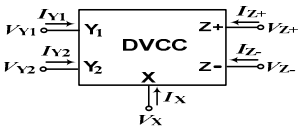

Fig. 1. Electrical symbol of DVCC.

II. CIRCUIT DESCRIPTION

The DVCC, whose electrical symbol is shown in Fig. 1, is a five-terminal analog building block and its terminal relations are given by [4]

The Y_1 and Y_2 terminals are high impedance terminals while X is low impedance terminal. The Z+ and Z- terminals are high impedance terminals suitable for current outputs.

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While the X terminal voltage follows the voltage difference of terminals Y_1 and Y_2. The current at terminal Z+ follows the current at terminal X in positive magnitude. The current at terminal Z- follows the current at terminal X in negative magnitude. The proposed first-order voltage-mode filter configuration comprises one DVCC, one grounded capacitor and one resistor, as shown in Fig. 2. The use of grounded capacitors makes the circuit suitable for integration because grounded capacitor circuit can compensate for the stay capacitances at their nodes [21]. Derived by each nodal equation of the proposed, the input-output relationship matrix form of Fig. 2 can be expressed as

$$\begin{bmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_{Z+} \\ V_{Z-} \end{bmatrix} \tag{1}$$

$$\begin{bmatrix} sC & G \\ -1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_o \end{bmatrix} = \begin{bmatrix} GV_{i2} \\ -V_{i1} \end{bmatrix} \tag{2}$$

where $G = \dfrac{1}{R}$

To derive (2), the Y_1 and Y_2 terminals of DVCC are high impedance terminals, since they are connected to gates of MOS devices in actual implementation, whereas the port X is low impedance terminal [4]. Similarly the ports Z+ and Z- also exhibit high impedance since they are connected to the output stage of current mirror. From (2), the output voltage V_o can be derived as

$$V_o = \frac{-sCRV_{i1} + V_{i2}}{sCR + 1} \tag{3}$$

The specialization of the numerator of this transfer function yields

(i) lowpass: $V_{i1} = 0$ and $V_{i2} = V_{in}$

(ii) highpass: $V_{i2} = 0$ and $V_{i1} = V_{in}$

(iii) allpass: $V_{i1} = V_{i2} = V_{in}$

Note that there is also no need of any component matching conditions and inverting type voltage input signals to realize all of the filter responses.

From (2), the first-order voltage-mode allpass filter response can be expressed as follows.

$$\frac{V_o}{V_{in}} = \frac{-sCR + 1}{sCR + 1} \tag{4}$$

The phase response of the first-order voltage-mode allpass filter can be expressed as

$$\varphi_o(\omega) = -2\arctan(\omega CR) \tag{5}$$

By taking into account the non-idealities of a DVCC, the relationship of the terminal voltages and current can be rewritten as

$$\begin{bmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & \beta_1 & -\beta_2 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \alpha_1 & 0 & 0 & 0 & 0 \\ -\alpha_2 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_{Z+} \\ V_{Z-} \end{bmatrix} \tag{6}$$

where $\alpha_i = 1 - e_i$ and e_i ($|e_i| << 1$) denote the current tracking error and $\beta_v = 1 - e_v$ and e_v ($|e_v| << 1$) denote the differential voltage tracking error. The first-order voltage-mode lowpass filter transfer function becomes

$$\frac{V_{LP}}{V_{in}} = \frac{\alpha_2\beta_1}{sCR + \alpha_2\beta_1} \tag{7}$$

The first-order voltage-mode highpass filter transfer function becomes

$$\frac{V_{HP}}{V_{in}} = \frac{-\beta_2 sCR}{sCR + \alpha_2\beta_1} \tag{8}$$

The first-order voltage-mode allpass filter transfer function becomes

$$\frac{V_{AP}}{V_{in}} = \frac{-\beta_2 sCR + \alpha_2\beta_1}{sCR + \alpha_2\beta_1} \tag{9}$$

The cutoff frequency ω_c is obtained by

$$\omega_c = \frac{\alpha_2\beta_1}{CR} \tag{10}$$

A sensitivity study forms an important index of the performance of any active network. The formal definition of sensitivity is

$$S_x^F = \frac{x}{F}\frac{\partial F}{\partial x} \tag{11}$$

where F represents ω_c and x represents any of the elements (R, C) or the active parameters (α_i , β_i). Based on the sensitivity expression, the active and passive sensitivities of the proposed circuit shown in Fig. 2 are given as

$$S_{\alpha_2}^{\omega_o} = S_{\beta_1}^{\omega_o} = 1 \tag{12}$$

$$S_R^{\omega_o} = S_C^{\omega_o} = -1 \tag{13}$$

Hence, the first-order filter parameter sensitivities of active and passive components for the pole ω_c of Fig. 2 are less than 1 in relative amplitude axis.

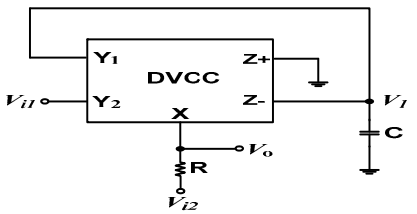

Fig. 2. The proposed DVCC-based first-order filter.

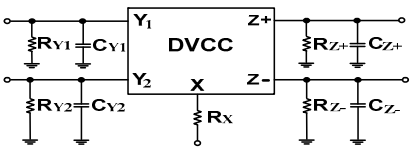

Fig. 3. DVCC symbol along with its parasitic elements.

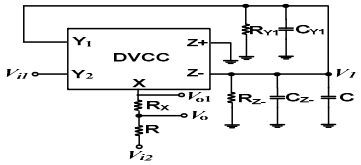

Fig. 4. The proposed DVCC-based first-order filter including parasitics.

III. Influence of Parasitic Elements

Equation (3) has been obtained by considering ideal description of DVCCs, all the two Y terminals exhibit an infinite input resistance. The port X exhibits zero input resistance and the ports Z show an infinite output resistance. Practically when implementing the active element using transistors, these resistances assume some finite value depending upon the device parameters. Similarly, the high frequency effects also need to be accounted for by assuming capacitances at these ports. The non-ideal DVCC symbol showing various parasitic is shown in Fig. 3. It is shown that the port X exhibits of low value parasitic serial resistance R_X, the ports Y exhibit of high value parasitic resistance R_Y in parallel with low value capacitance C_Y, and the ports Z exhibit of high value parasitic resistance R_Z in parallel with low value capacitance C_Z. It is to be noted that the proposed circuit employs resistors at X terminals of the DVCCs, hence most of the parasitics R_X can be easily merged. To account for these non-ideal sources, the proposed circuit in Fig. 2 can be redrawn as Fig. 4. Reanalysis of the proposed circuit, the input-output relationship matrix form of Fig. 4 can be rewritten as follows.

$$\begin{bmatrix} s & n \\ -1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_{o1} \end{bmatrix} = \begin{bmatrix} nV_{i2} \\ -V_{i1} \end{bmatrix} \tag{14}$$

where

$$n = \left(\frac{1}{R'C'}\right)\left(\frac{s}{s+\omega_p}\right) \quad , \quad \omega_p = \frac{1}{R_p C'} \quad C' = C + C_{Z-} + C_{Y1} \quad ,$$

$$R_p = R_{Z-} // R_{Y1} \text{, and } R' = R + R_{X+} \tag{15}$$

From (14), the non-idealities of the output voltage V_o can be derived as

$$V_{o1} = \frac{-sV_{i1} + nV_{i2}}{s+n} \tag{16}$$

Equation (16) illustrate that the effects of the parasitic elements are dependent on a parasitic pole yielded by the non-idealities of the DVCC. For close to ideal operation at high frequencies, the frequency of operation should be larger than ω_p. Thus, the frequency range of the proposed configuration should be restricted to the following conditions [22].

$$10 f_p \le f \tag{17}$$

It is not difficult to satisfy this condition, since the external capacitance can be chosen to be much greater than parasitic capacitance. For example, if the proposed circuit was designed for f_o=1.59MHz by choosing R=10kΩ and C=10pF and R_X=150.2Ω, R_{Z+}=5.03MΩ, C_{Z+}=0.024pF, R_{Z-}=5.3MΩ, C_{Z-}=0.031pF, $C_{Y1}=C_{Y2}$=3.86fF (as simulated in the next section), then the parasitic pole f_P will be located at approximately 2.992kHz. Thus, the ideal operation will be valid for frequencies higher than approximately 10 f_P. If the useful frequency range of the proposed filter is limited in (17), the influences of parasitic elements to the coefficient n will be diminished. Therefore, the voltage transfer response in (16) can be rewritten as

It is to be noted that the resistor of the proposed filter is connected to the X terminals of the DVCCs and the capacitor of the proposed filter is connected to the Y or Z terminals. Thus all the loading effects of the parasitics can be accommodated.

$$V_o = \frac{-sV_{i1} + \frac{1}{R'C'}V_{i2}}{s + \frac{1}{R'C'}} \tag{18}$$

IV. Simulation Results

The device model parameters used for HSPICE simulations are TSMC 0.18 μm 1P6M CMOS process technology and Matlab for the theoretical part to compare the results. The CMOS implementation of a DVCC is shown in Fig. 5 [9]. The aspect ratios of the CMOS transistors of the DDCC are shown in Table I. The supply voltages are V_{DD}=-V_{SS}=0.9V, and the biasing voltages are V_{B1}=-0.1V and V_{B2} =-0.36V. The voltage follower and current follower frequency responses of DVCC are, respectively, shown in Figs. 6 and 7 which are obtained more than 100MHz. The f_{-3dB} frequencies for the voltage and current transfers are summarized in Table II. The frequency response of the output impedances of the DVCC is shown in Fig. 8. It can be seen that the port *Z+ of DVCC* exhibits of high value parasitic resistance R_{Z+} *(5.03MΩ)* in parallel with low value capacitance C_{Z+} *(0.024pF),* and the port Z- exhibits of high value parasitic resistance R_{Z-} *(5.3MΩ)* in parallel with low value capacitance C_{Z-} *(0.031pF)*. Thus, the parasitic capacitance of the circuit has a small value that can be neglected in our frequency range of interest. The frequency response of the input impedance of the DVCC is shown in Fig. 9. It can be seen that the port X of DVCC exhibits of low value parasitic resistance R_X *(150.2Ω)* in series with low parasitic inductance L_X *(4.16μH*), which makes it suitable for cascading. The parasitic elements of the DVCC have been calculated in Table III.

The allpass filter phase shifter was designed for a 90^o phase shift at f_c=1.59MHz. The component values of Fig. 2 are given by R=10kΩ and C=10pF. Figs. 10 and 11 show the simulated results of the lowpass gain and phase plot of Fig. 2 with $V_{i2}=V_{in}$ and $V_{i1}=0$. Figs. 12 and 13 show the simulated results of the highpass gain and phase plot of Fig. 2 with $V_{i1}=V_{in}$ and $V_{i2}=0$. Figs. 14 and 15 show the simulated results of the allpass gain and phase plot of Fig. 2 with $V_{i1}=V_{i2}=V_{in}$. It is observed from Figs. 10 to 15 that the simulation results agree quite well with the theoretical analysis, but the difference between the theoretical and simulated responses mainly stems from the parasitic impedance effects and non-ideal gains of the DVCC.

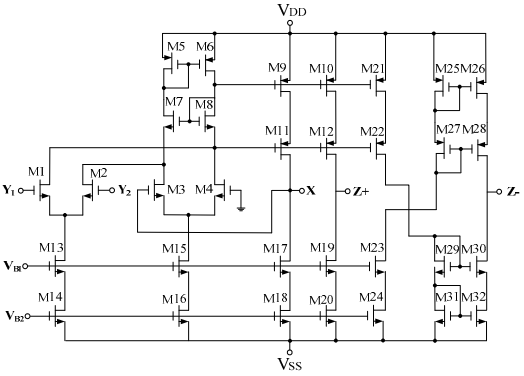

Fig. 5. The CMOS implementation of the DVCC.d

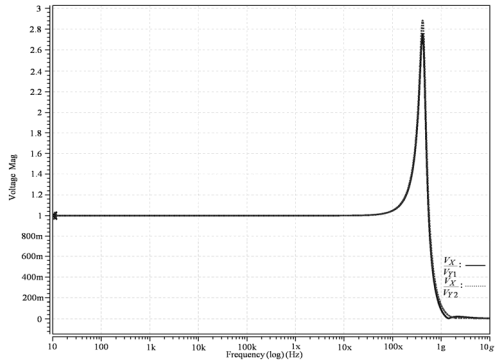

Fig. 6. Frequency response of X terminal with respect to different Y terminals.

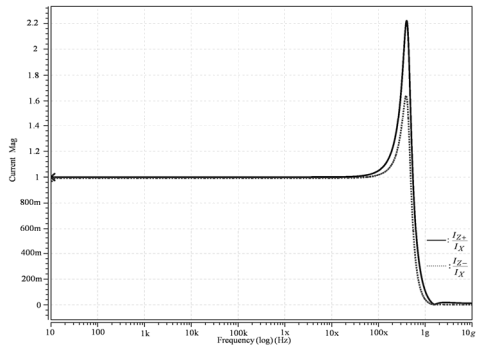

Fig. 7. Frequency response of Z+/Z- terminals with respect to X terminal.

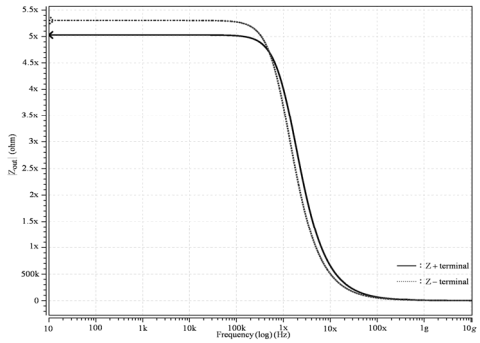

Fig. 8. Magnitude of the parasitic output impedances at Z+ and Z- terminals.

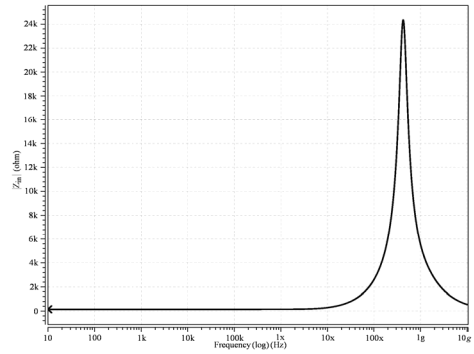

Fig. 9. Magnitude of the parasitic input impedance at X terminal.

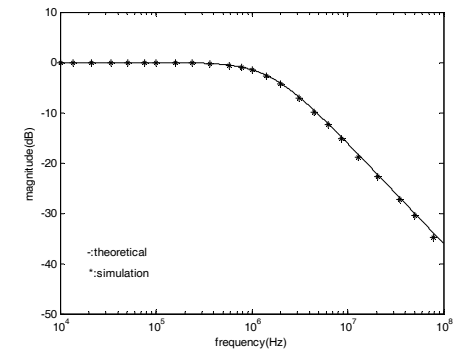

Fig. 10. Amplitude-frequency response of lowpass filter at f_c=1.59MH$_Z$.

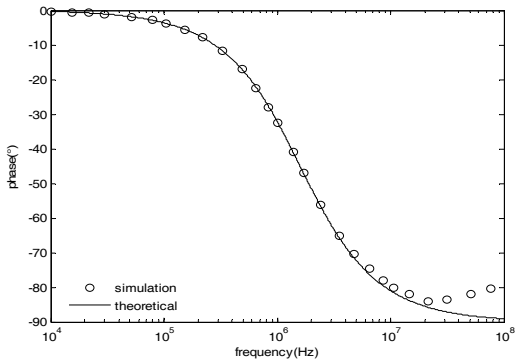

Fig. 11. Phase response of lowpass filter at f_c=1.59MH$_Z$.

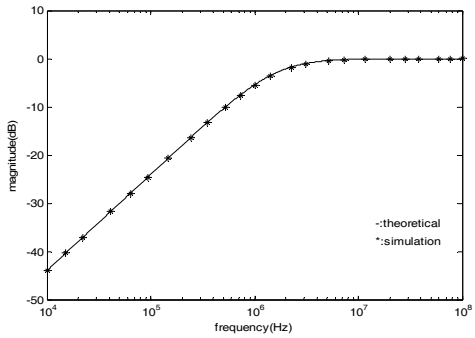

Fig. 12. Amplitude-frequency response of highpass filter at f_c=1.59MH$_Z$.

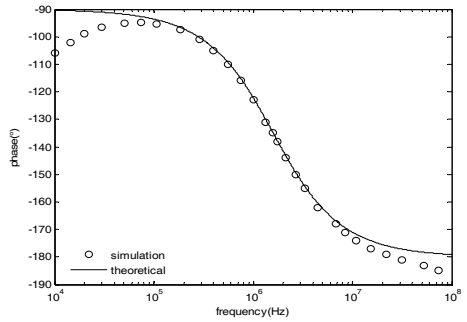

Fig. 13. Phase response of highpass filter at f_c=1.59MH$_Z$.

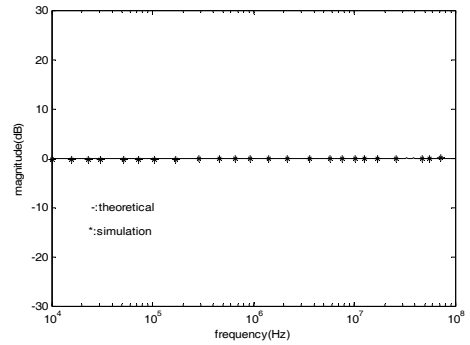

Fig. 14. Amplitude-frequency response of allpass filter at f_c=1.59MH$_Z$.

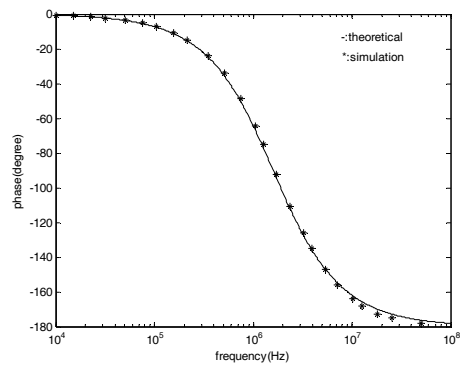

Fig. 15. Phase response of allpass filter at f_c=1.59MH$_Z$.

TABLE I. THE ASPECT RATIOS OF THE CMOS TRANSISTORS IN DVCC IMPLEMENTATION.

Transistors	L(μm)	W(μm)
M1—M4	0.36	3.6
M7—M8	0.36	5.4
M13—M20, M23—M24	0.18	2.52
M5—M6, M9—M12, M21—M22	0.18	10.08
M25—M28	0.36	12.6
M29 —M32	0.36	7.92

TABLE II. VOLTAGE AND CURRENT TRANSFERS WITH F-3DB FREQUENCIES.

Transfer	DC gain	f_{-3dB}MHz
V_X/V_{Y1}	1.0000	588.84
V_X/V_{Y2}	0.9999	605.86
I_{Z+}/I_X	0.9999	598.4
I_Z/I_X	0.9994	529.2

TABLE III. PARASITIC COMPONENT VALUES OF THE DVCC.

Parasitic	Value
R_X	150.2Ω
L_X	4.16μH
C_{Y1}	3.86fF
C_{Y2}	3.86fF
R_{Z+}	5.03MΩ
C_{Z+}	0.024pF
R_{Z-}	5.3MΩ
C_{Z-}	0.031pF

V. CONCLUSIONS

In this paper, a new first-order grounded-capacitor voltage-mode filter employing minimum active and passive components is proposed. The proposed configuration employs one DVCC, one grounded capacitor and one resistor and still has the following advantages: employment of only one current conveyor, employment of only one grounded capacitor, employment of only one resistor, simultaneous realization of voltage-mode first-order lowpass, highpass and allpass filter responses from the same configuration, no need to impose component choice conditions, and low active and passive sensitivity performances. HSPICE simulation results using TSMC 0.18 μm 1P6M CMOS process technology and ±0.9V supply voltages validate the theoretical predictions.

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