MODIFIED DUAL-CLCG METHOD AND ITS VLSI ARCHITECTURE FOR PSEUDORANDOM GENERATION

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Abstract**—**In modern digital communication and VLSI systems, the generation of high quality pseudorandom sequences plays a crucial role in ensuring data security, efficient encoding, and reliable transmission. This paper presents a Modified Dual Combined Linear Congruential Generator method along with its efficient VLSI architecture for pseudorandom number generation.The proposed approach enhances the statistical quality and randomness properties compared to conventional generators by combining two linear congruential sequences in a modified structure. This dual mechanism reduces correlation, improves periodicity, and ensures better uniform distribution of generated sequences, making it suitable for applications such as cryptography, communication systems, and error-control coding.

Keywords— Pesudorandom Number Generator, Dual CLCG, Modified Dual CLCG, VLSI Architecture, FPGA Implementation, Verilog HDL, Parallel Processing, Random Sequence Generation, Digital Communication, Hardware Optimization, Low Power Design, High Throughput Systems.

I. INTRODUCTION

In today's digital era, the demand for secure, high-speed, and reliable communication systems has increased significantly. One of the key components that supports such systems is the generation of high-quality pseudorandom sequences, which are widely used in applications such as cryptography, wireless communication, error correction, and simulation models. The effectiveness of these applications largely depends on the randomness, periodicity, and statistical properties of the generated sequences.

Traditional pseudorandom number generators, particularly Linear Congruential Generators (LCGs), are simple and efficient but suffer from limitations such as short periods and predictable patterns. To overcome these drawbacks, combined and modified generator techniques have been introduced. Among them, the Dual Combined Linear Congruential Generator (Dual-CLCG) improves randomness by combining two independent sequences. However, further enhancement is still required to meet the demands of modern high-performance systems.

In this work, a Modified Dual-CLCG method is proposed to improve the statistical quality and randomness characteristics of generated sequences. The modification focuses on reducing correlation between sequences, increasing the period, and achieving a more uniform distribution. This makes the proposed generator more suitable for advanced digital systems where reliability and unpredictability are critical.

Along with algorithmic improvement, efficient hardware implementation is equally important. With the rapid advancement of Very Large Scale Integration (VLSI) technology, complex digital systems can now be integrated onto a single chip with high performance and low power consumption. In this project, the proposed Modified Dual-CLCG is designed using Verilog HDL and implemented on

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an FPGA platform. Special emphasis is given to parallel architecture, which significantly reduces processing time and enhances throughput compared to conventional serial approaches.

The results demonstrate that the proposed design achieves improved performance in terms of speed, area utilization, and efficiency, making it a suitable candidate for real-time and embedded applications. This work contributes to the development of optimized pseudorandom generators that can be effectively integrated into modern VLSI-based systems.

II. REVIEW&LITERATURE SURVEY

The design of efficient pseudorandom generators and high-performance encoding architectures has been an active area of research in digital communication and VLSI systems. Various techniques have been proposed to improve randomness quality, throughput, and hardware efficiency.

Early work in coding techniques focused on improving transmission reliability using advanced modulation and encoding schemes such as Trellis Coded Modulation (TCM). These techniques enhance error performance without increasing bandwidth by maximizing the Euclidean distance between signal points. Later, the combination of TCM with turbo coding methods demonstrated significant improvements in communication reliability, especially in high-speed and optical communication systems.

Turbo codes have gained widespread attention due to their near-Shannon limit performance in error correction. Several architectures for turbo decoders have been developed to achieve high throughput. However, implementing turbo decoding algorithms in hardware introduces challenges such as high complexity, increased power consumption, and large silicon area. To address these issues, researchers have proposed optimized architectures like Log-BCJR and Max-Log-BCJR algorithms, which reduce computational complexity while maintaining acceptable decoding performance.

In recent years, Application-Specific Instruction Set Processors (ASIP) and Network-on-Chip (NoC) based architectures have been explored for turbo decoder implementation. These approaches aim to provide flexibility and scalability while supporting high data rates. Although they improve throughput, they often introduce additional complexity and resource overhead. To overcome these limitations, simplified architectures using finite state machine (FSM) approaches have been proposed to reduce design complexity and improve efficiency.

Parallel processing has also been widely investigated as a solution for achieving higher throughput in communication systems. In standards such as LTE, parallel turbo decoder architectures have been developed to support data rates exceeding hundreds of Mbps. These architectures utilize multiple processing units working simultaneously, but they require efficient memory access techniques to avoid conflicts, leading to the development of contention-free interleavers.

From a hardware perspective, FPGA-based implementations have become popular due to their flexibility, reconfigurability, and reduced development cost. Several studies have demonstrated that parallel architectures implemented on FPGA platforms can significantly improve performance metrics such as speed and resource utilization compared to serial designs.

Despite these advancements, traditional pseudorandom generation techniques like basic LCGs still suffer from limitations in randomness quality and predictability. Even combined generators require further enhancement to meet the increasing demands of secure and high-speed systems. Therefore, there is a need for improved methods that not only enhance randomness properties but also provide efficient hardware implementation.

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Motivated by these challenges, this work proposes a Modified Dual-CLCG method along with an optimized VLSI architecture. The proposed approach focuses on improving randomness quality while reducing hardware complexity and increasing processing efficiency through parallel design techniques.

III. RESEARCH METHODOLOGY

The proposed work focuses on the design and implementation of a Modified Dual-CLCG based pseudorandom generator along with an efficient VLSI architecture. The methodology is structured in a systematic manner, starting from algorithm development to hardware realization and performance evaluation.

3.1 Design of Modified Dual-CLCG Algorithm

The foundation of this research lies in enhancing the conventional Linear Congruential Generator (LCG) by combining two independent generators to form a Dual-CLCG. Each generator produces a sequence based on modular arithmetic, and the outputs are combined using a modified approach to improve randomness.

The proposed modification introduces:

- Improved seed initialization to avoid repetition patterns
- Enhanced combination logic to reduce correlation between sequences
- Increased periodicity for better statistical performance

This ensures that the generated pseudorandom sequence has better uniform distribution and unpredictability compared to traditional methods.

3.2 Mathematical Modeling

Each LCG is defined using a recurrence relation of the form:

Xn+1=(aXn+c)mod mX_{n+1} = (aX_n + c) \mod mXn+1=(aXn+c)modm

In the proposed method, two such sequences are generated in parallel and combined using a carefully designed function. The modification ensures that the resulting sequence overcomes the limitations of single LCGs such as short period and linear predictability.

3.3 Hardware Architecture Design

To implement the proposed algorithm efficiently, a hardware architecture is designed using Verilog HDL. The architecture consists of:

- Two independent LCG modules
- A combination unit for merging outputs
- Control logic for synchronization
- Registers for storing intermediate values

The design is optimized to support both serial and parallel computation techniques, with emphasis on parallel execution to enhance performance.

3.4 FPGA Implementation

The designed architecture is implemented on an FPGA platform using industry-standard tools. The process includes:

- RTL design and coding in Verilog
- Functional simulation using test benches
- Synthesis and implementation on FPGA
- Resource utilization and timing analysis

Parallel processing is employed to reduce computation time significantly, similar to improvements observed in encoding architectures .

3.5 Performance Evaluation

The performance of the proposed system is evaluated based on:

- Randomness quality (uniformity and distribution)
- Hardware utilization (LUTs, flip-flops)
- Processing speed and latency
- Power efficiency

Comparative analysis is performed between conventional methods and the proposed Modified Dual-CLCG to highlight improvements in both algorithmic performance and hardware efficiency.

IV. EXSITING SYSTEM

In conventional digital systems, pseudorandom number generation is primarily implemented using simple algorithms such as the Linear Congruential Generator (LCG). Due to its ease of implementation and low computational complexity, LCG has been widely used in applications like simulations, communication systems, and basic cryptographic processes.

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The LCG generates a sequence using a linear recurrence relation based on modular arithmetic. Although it is efficient in terms of hardware and execution speed, it suffers from several inherent limitations. The generated sequences often exhibit short periods, predictable patterns, and poor statistical randomness, especially when used in high-security or high-performance applications.

To improve the performance, Combined Linear Congruential Generators (CLCG) and Dual-CLCG methods were introduced. These systems use two or more LCGs whose outputs are combined to enhance randomness and extend the period. While this approach improves performance compared to a single LCG, it still faces challenges such as:

- Residual correlation between generated sequences
- Increased hardware complexity
- Limited optimization in conventional architectures
- Inefficient utilization of parallel processing capabilities

From a hardware perspective, many existing implementations are based on serial computation techniques, where operations are performed sequentially. This leads to higher processing time and limits throughput, making them less suitable for real-time and high-speed applications. Additionally, traditional architectures may consume more power and area when scaled for higher performance requirements.

In FPGA-based implementations, although flexibility is achieved, the lack of optimized architectural design results in inefficient resource utilization and longer execution times. As highlighted in prior work, serial processing approaches significantly increase computation cycles, whereas parallel techniques can greatly enhance performance .

Due to these limitations, existing systems are not fully capable of meeting the demands of modern applications such as secure communication, high-speed data processing, and advanced VLSI systems.

V. PROPOSED METHODOLOGY

The proposed methodology presents a Modified Dual-CLCG (Combined Linear Congruential Generator) approach for generating high-quality pseudorandom sequences, along with an efficient VLSI-based hardware architecture. The design aims to overcome the inherent limitations of conventional pseudorandom generators such as short period, linearity, and predictability. In this method, two independent LCG units are employed, each generating a sequence using modular arithmetic with carefully selected parameters including multiplier, increment, and modulus. Unlike traditional dual-generator approaches, the proposed system introduces a modified combination mechanism that effectively reduces correlation between the two sequences and enhances statistical randomness. Additionally, improved seed initialization techniques are used to avoid repetition and ensure better distribution of output values over a longer period.

A key feature of the proposed system is the adoption of a parallel processing architecture, where both LCG units operate simultaneously rather than sequentially. This parallelism significantly reduces computation time and increases throughput, making the design suitable for high-speed and real-time applications. The architecture consists of two LCG modules, a dedicated combination unit for merging outputs, control logic for synchronization, and registers for intermediate data storage. The combination unit is carefully designed to preserve randomness properties while maintaining low hardware complexity. By executing multiple operations within a single clock cycle, the system achieves faster processing compared to conventional serial implementations, which typically require multiple clock cycles for similar operations.

The entire system is modeled using Verilog Hardware Description Language (HDL) at the register transfer level (RTL) and implemented on an

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FPGA platform. The design flow includes coding, functional simulation using test benches, synthesis, and hardware mapping. FPGA implementation provides advantages such as flexibility, reconfigurability, and rapid prototyping, making it an ideal choice for validating the proposed architecture. Special attention is given to optimizing hardware resources such as lookup tables (LUTs), flip-flops, and routing paths to ensure efficient utilization of the device.

Furthermore, the proposed design focuses on performance optimization in terms of speed, area, and power consumption. The use of parallel architecture reduces latency and improves overall system efficiency, while optimized logic design minimizes hardware usage and switching activity, leading to lower power consumption. The methodology also ensures scalability, allowing the design to be extended for higher bit-widths or integrated into larger VLSI systems without significant overhead.

The performance of the proposed Modified Dual-CLCG system is evaluated through simulation and synthesis results, which demonstrate improved randomness characteristics, reduced processing time, and efficient resource utilization compared to existing methods. These improvements make the proposed architecture highly suitable for applications such as cryptographic systems, secure communications, digital signal processing, and other real-time embedded systems where reliable and high-speed pseudorandom generation is essential.

VI. BLOCK DIAGRAM

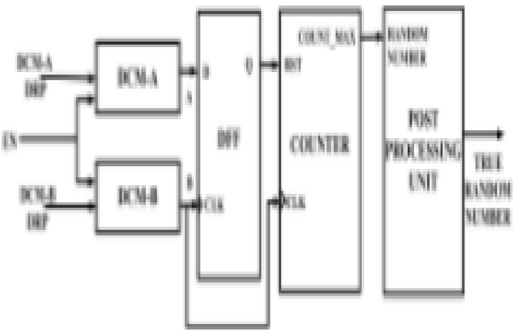

Fig. 6.2. Block Diagram

VII. RESULTS AND OUTCOMES

The proposed Modified Dual-CLCG based pseudorandom generator was successfully designed, verified through simulation, and implemented on an FPGA platform using Verilog HDL, and the obtained results clearly demonstrate improvements in both randomness quality and hardware performance. The simulation results indicate that the generated sequences exhibit enhanced statistical characteristics such as improved uniform distribution, reduced correlation between successive values, and increased periodicity. These properties confirm that the proposed modification effectively overcomes the limitations of conventional LCG and basic combined generators, making the output sequence more suitable for secure and high-reliability applications.

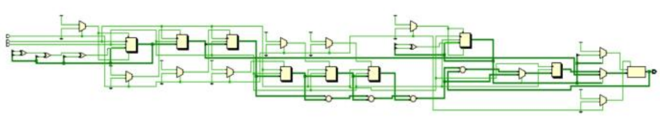

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Fig:7.1: Output1

From the hardware implementation perspective, the use of a parallel processing architecture plays a significant role in improving system performance. Unlike traditional serial approaches, where operations are executed sequentially over multiple clock cycles, the proposed design performs multiple computations simultaneously, thereby significantly reducing execution time and latency. As a result, the system achieves higher throughput and faster response, which is essential for real-time digital systems. Similar improvements in processing efficiency due to parallel computation have also been reported in FPGA-based designs, where processing time can be considerably reduced while maintaining accuracy .

Utilization — Post-Synthesis | **Post-Implementation**

Graph | **Table**

Resource	Utilization	Available	Utilization %
LUT	44	53200	0.08
FF	100	106400	0.09
IO	19	200	9.50
BUFG	1	32	3.13

Fig:7.2:Output 2

In terms of resource utilization, the synthesis results show that the proposed architecture efficiently uses FPGA resources such as lookup tables (LUTs), flip-flops, and routing elements. The design minimizes redundant logic and ensures optimal utilization of available hardware, leading to a compact implementation with reduced chip area. Additionally, the optimized logic structure contributes to lower switching activity, which in turn reduces overall power consumption. This makes the proposed system particularly suitable for power-constrained applications such as embedded systems and portable electronic devices.

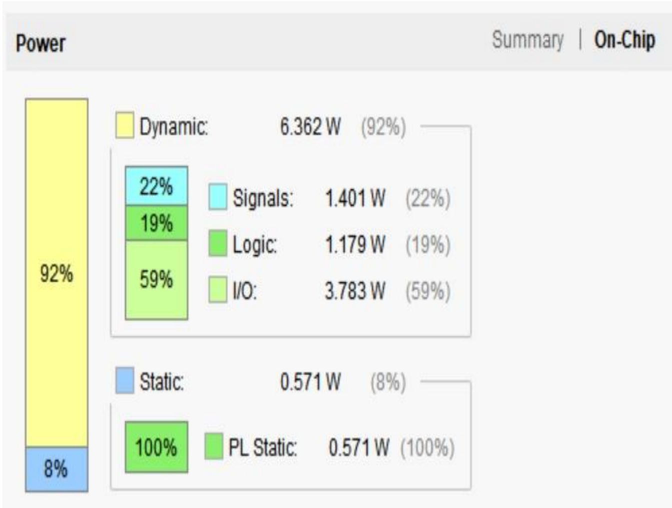

Fig:7.3:Output 3

Another important outcome of this work is the scalability and flexibility of the design. The modular architecture allows easy extension to higher bit-widths or integration into larger VLSI systems without significant redesign effort. Moreover, the use of FPGA technology provides reconfigurability, enabling the system to be adapted for different applications and performance requirements.

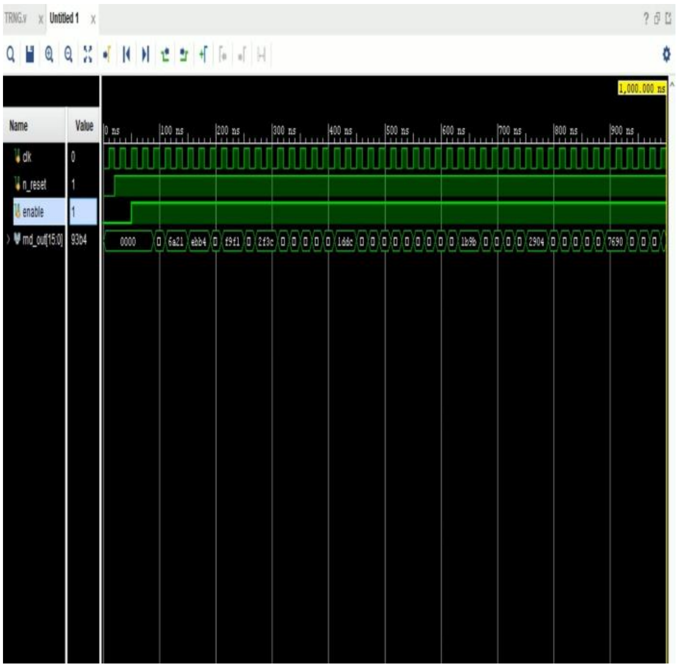

Fig:7.4: Output 4

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Overall, the results confirm that the proposed Modified Dual-CLCG architecture achieves a strong balance between performance, hardware efficiency, and randomness quality. The improvements in speed, reduced processing time, optimized area utilization, and lower power consumption make the design highly effective for applications such as cryptographic systems, secure communications, digital signal processing, and other real-time VLSI-based implementations where reliable pseudorandom number generation is essential.

VIII. CONCLUSION

In this work, a Modified Dual-CLCG method along with an efficient VLSI architecture for pseudorandom number generation has been successfully designed, implemented, and evaluated. The proposed approach addresses the major limitations of conventional pseudorandom generators, such as short period, predictability, and correlation, by combining two LCG units with an improved modification technique. This modification enhances the statistical quality of the generated sequences, resulting in better uniformity, increased periodicity, and improved randomness characteristics, which are essential for modern digital and secure communication systems.

The hardware realization of the proposed system using Verilog HDL and FPGA technology demonstrates the practicality and effectiveness of the design. By adopting a parallel processing architecture, the system achieves a significant reduction in processing time and latency compared to traditional serial implementations. This leads to higher throughput and improved overall system performance. Additionally, the design ensures efficient utilization of hardware resources such as lookup tables and flip-flops, thereby reducing chip area and power consumption. These improvements highlight the suitability of the proposed architecture for real-time and embedded applications where both speed and efficiency are critical.

Another important contribution of this work is the balance achieved between algorithmic enhancement and hardware optimization. While the modified Dual-CLCG improves randomness quality at the algorithm level, the parallel VLSI architecture ensures that these improvements are realized efficiently in hardware. The modular and scalable nature of the design further enables easy integration into larger VLSI systems and adaptation to different application requirements.

Overall, the results validate that the proposed Modified Dual-CLCG architecture provides a robust, high-performance, and resource-efficient solution for pseudorandom number generation. It is well suited for applications in cryptography, digital communication, signal processing, and other advanced VLSI-based systems. Future work can focus on extending this design by incorporating advanced randomness testing, exploring ASIC-level implementation, and further optimizing power and area for next-generation high-speed applications.

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