High Performance Multiply-Accumulate Unit By Integrating Additions And Accumulations Into Partial Product Reduction Process

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***Abstract*—The multiply–accumulate (MAC) unit is a fundamental computational block widely used in digital signal processing (DSP), artificial neural networks (ANNs), and modern high-performance computing systems. The efficiency of these systems heavily depends on the speed, area, and power consumption of the MAC unit. Conventional MAC architectures typically implement multiplication and accumulation as separate operations, which introduces additional delay due to intermediate additions and carry propagation, thereby affecting overall system performance.This work presents a high-performance MAC unit by integrating addition and accumulation operations directly into the partial product reduction process. By embedding accumulation within the multiplication stage, the proposed architecture reduces redundant operations and shortens the critical path delay. The design utilizes optimized techniques such as modified Booth encoding, efficient partial product generation, and advanced reduction strategies to enhance computational efficiency.Furthermore, the proposed approach minimizes hardware complexity and power consumption by reducing the number of accumulation stages and eliminating unnecessary correction terms during partial product reduction in delay, area, and power metrics compared to conventional**

Keywords— Multiply-Accumulate (MAC), Partial Product Reduction, Booth Encoding, VLSI, DSP, Neural Networks, Verilog HDL.

I. INTRODUCTION

The rapid advancement of digital systems, particularly in areas such as digital signal processing (DSP), artificial intelligence, and machine learning, has significantly increased the demand for high-performance arithmetic units. Among these, the multiply–accumulate (MAC) unit plays a crucial role, as it forms the computational backbone of many applications including filtering, image processing, and neural network operations. In modern architectures such as convolutional neural networks (CNNs), a large portion of computation time is dominated by repeated MAC operations, making their optimization essential for improving overall system performance.

Conventional MAC unit designs typically perform multiplication and accumulation as two separate sequential operations. The multiplication stage generates partial products, which are then summed using adders before being accumulated. This separation introduces additional delay due to carry propagation and intermediate storage, resulting in increased latency, higher power consumption, and larger silicon area. As system complexity grows, these limitations become more significant, particularly in real-time and low-power applications.

To address these challenges, recent research has focused on optimizing the internal structure of MAC units, especially the partial product generation and reduction stages. Techniques such as modified Booth encoding, carry-save adders, and Vedic multiplication methods have been explored to improve speed and efficiency. However, many existing approaches still treat addition and accumulation as separate processes, leaving room for further optimization.

In this work, a high-performance MAC unit is proposed by integrating addition and accumulation directly into the partial product reduction process. By fusing these operations, the design reduces redundant computations and minimizes the critical path delay. The proposed architecture also aims to improve area and power efficiency while maintaining high computational throughput. The design is implemented using hardware description language (Verilog HDL) and evaluated through simulation and synthesis to demonstrate its effectiveness over conventional approaches.

II. REVIEW LITERATURE SURVEY

The design of high-performance multiply–accumulate (MAC) units has been an active area of research due to their critical role in digital signal

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processing (DSP) and neural network applications. Various architectures and optimization techniques have been proposed to enhance speed, reduce power consumption, and minimize hardware complexity.

Several researchers have explored neural network hardware acceleration using configurable architectures. A CORDIC-based reconfigurable neuron design was proposed to support both MAC operations and activation functions within a single hardware block, improving flexibility and resource utilization. However, such designs often involve increased structural complexity.

Multiplier design plays a significant role in MAC unit performance. Modified Booth encoding techniques have been widely adopted to reduce the number of partial products, thereby improving multiplication speed. Advanced radix-4 and higher radix Booth encoders further enhance performance by minimizing computational steps. However, these approaches introduce additional encoding logic, which may increase area overhead.

Vedic multiplication techniques, particularly the UrdhvaTiryagbhyam method, have gained attention due to their parallelism and reduced delay characteristics. Researchers have demonstrated that Vedic multipliers outperform conventional array multipliers in terms of speed, making them suitable for high-speed MAC units. Nevertheless, their efficiency depends on the effectiveness of the associated adder circuits.

Adder architectures also significantly impact MAC performance. The Square Root Carry Select Adder (SQRT-CSLA) has been proposed as a faster alternative to ripple carry adders, offering reduced delay with moderate area increase. Binary-to-Excess-1 Converter (BEC)-based CSLAs further optimize area while maintaining speed advantages.

In addition, redundant binary (RB) and carry-save techniques have been used to improve partial product reduction. Recent studies introduced modified partial product generators that eliminate extra correction terms and reduce accumulation stages, leading to improvements in delay, area, and power consumption . These approaches highlight the importance of optimizing the reduction stage for overall MAC efficiency.

Furthermore, fused add-multiply (FAM) architectures have been proposed to combine addition and multiplication into a single data path. By eliminating intermediate addition stages, these designs reduce critical path delay and improve computational efficiency. However, their implementation complexity and hardware overhead remain challenges.

Despite these advancements, most existing MAC architectures still treat multiplication and accumulation as separate operations. This separation leads to increased latency and redundant computations. Therefore, there is a need for a more integrated approach that combines addition and accumulation within the partial product reduction process.

The proposed work addresses these limitations by introducing a high-performance MAC unit that integrates additions and accumulations directly into the partial product reduction stage. This approach aims to reduce delay, minimize hardware complexity, and improve overall system efficiency.

III. RESEARCH METHODOLOGY

This research follows a structured and analytical methodology to design a high-performance multiply–accumulate (MAC) unit by integrating addition and accumulation operations into the partial product reduction process. The study begins with an in-depth investigation of conventional MAC architectures used in digital signal processing (DSP) and neural network accelerators. Existing designs typically rely on separate stages for multiplication and accumulation, where partial products are generated, summed using multi-stage adders, and then accumulated. Although widely used, these architectures suffer from increased latency due to carry propagation, higher power consumption, and larger silicon area requirements . This initial analysis helps identify the critical bottlenecks in the multiplication and accumulation pipeline.

Based on the limitations identified, the proposed methodology introduces a novel architectural approach that combines addition and accumulation directly within the partial product reduction stage. Instead of performing accumulation after the multiplication process, the accumulation operation is embedded into the reduction tree, enabling simultaneous execution of multiplication and accumulation. This fusion reduces redundant intermediate additions and eliminates the need for separate accumulation hardware. Additionally, optimized encoding techniques such as

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Modified Booth encoding are considered to reduce the number of partial products, thereby decreasing computational complexity and improving speed.

To further enhance performance, efficient partial product reduction techniques are employed. Carry-save and redundant binary representations are explored to minimize carry propagation delays during intermediate stages. By reducing the number of accumulation levels and eliminating unnecessary correction terms, the proposed method achieves a shorter critical path and improved throughput. The architecture is also designed to support pipelining, allowing multiple operations to be processed concurrently, which significantly increases the processing speed in real-time applications.

The implementation phase involves modeling the proposed MAC unit using Verilog HDL. The design is divided into modular components, including partial product generation, reduction logic, and integrated accumulation blocks. Each module is individually tested and verified to ensure correctness before system-level integration. Functional simulation is carried out using tools such as ModelSim, while synthesis and performance analysis are performed using platforms like Xilinx or Synopsys Design Compiler. Timing analysis, area utilization, and power estimation are obtained to evaluate the effectiveness of the design.

To validate the proposed methodology, a comparative analysis is conducted against existing MAC architectures. Key performance metrics such as propagation delay, power consumption, area utilization, and power-delay product (PDP) are measured. The results demonstrate that the integration of addition and accumulation into the partial product reduction process significantly reduces delay and improves efficiency. Furthermore, the reduction in hardware complexity contributes to lower power consumption and optimized area usage.

Overall, this methodology provides a comprehensive framework for designing high-speed and energy-efficient MAC units. By focusing on architectural optimization, efficient arithmetic techniques, and hardware-level implementation, the proposed approach addresses the limitations of traditional designs and offers a scalable solution suitable for advanced DSP systems, neural network accelerators, and VLSI applications.

IV. EXISTING SYSTEM

The existing multiply–accumulate (MAC) unit architectures are primarily designed using a combination of conventional multipliers and adders, where multiplication and accumulation are performed as two distinct operations. In a typical design, the multiplication process is carried out first using techniques such as array multipliers or Modified Booth multipliers, followed by the addition of the product to an accumulator using carry-propagate adders. This sequential execution increases the overall computation time, as each stage depends on the completion of the previous one.

In these systems, partial products are generated based on the multiplier bits and then summed using multi-stage adder structures such as ripple carry adders, carry look-ahead adders, or carry save adders. Although carry save techniques help reduce intermediate carry propagation delay, the final addition stage still introduces significant latency. Furthermore, Modified Booth encoding is often used to reduce the number of partial products, but it requires additional encoding and correction logic, which increases design complexity.

Another limitation of the existing MAC units is the presence of multiple accumulation stages. After partial product reduction, the result must pass through a final adder before being accumulated, leading to increased critical path delay. In many designs, error correction terms are also introduced during partial product generation and reduction, which further increases the number of computation stages and hardware resources . As a result, the system consumes more power and occupies larger silicon area.

Additionally, conventional architectures do not efficiently utilize parallelism between multiplication and accumulation operations. Since accumulation is performed only after multiplication is completed, the opportunity for overlapping computations is lost. This limitation becomes more critical in high-speed applications such as digital signal processing and neural network implementations, where a large number of MAC operations are required continuously.

Overall, while existing MAC architectures provide acceptable performance for basic applications, they suffer from key drawbacks including high delay, increased power consumption, larger area, and inefficient utilization of computational resources. These limitations highlight the need for an improved architecture that integrates addition and accumulation within the multiplication process to achieve better performance and efficiency.

V. PROPOSED METHODOLOGY

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The proposed system presents a high-performance multiply–accumulate (MAC) unit that integrates addition and accumulation operations directly into the partial product reduction process. Unlike conventional architectures where multiplication and accumulation are performed sequentially, the proposed design fuses these operations into a unified computation flow. This integration significantly reduces redundant intermediate steps and minimizes the overall computation delay.

In the proposed architecture, partial products are generated using an optimized encoding technique such as Modified Booth encoding or efficient multiplier structures. Instead of summing these partial products separately and then passing the result to an accumulator, the accumulation process is embedded within the reduction tree itself. This means that the intermediate sums generated during partial product reduction are directly combined with the accumulated value, eliminating the need for a separate accumulation stage.

A key feature of the proposed system is the use of an optimized partial product reduction technique that reduces the number of accumulation levels. By eliminating extra correction terms and merging them within the reduction process, the design decreases both the hardware complexity and critical path delay . Additionally, carry-save or redundant arithmetic techniques are employed to reduce carry propagation delays during intermediate stages, further improving speed.

To enhance performance, the architecture supports pipelining, allowing multiple MAC operations to be processed simultaneously at different stages. This increases throughput and makes the system suitable for high-speed applications such as DSP and neural network accelerators. The design also focuses on power and area efficiency by reducing the number of logic gates and avoiding unnecessary intermediate storage elements.

The proposed MAC unit is implemented using Verilog HDL and verified through simulation and synthesis. The modular design approach ensures flexibility and scalability for different word lengths and applications. Performance evaluation shows that the proposed system achieves reduced delay, lower power consumption, and improved area utilization compared to conventional MAC architectures.

Overall, by integrating addition and accumulation into the partial product reduction process, the proposed system provides a faster, more efficient, and scalable solution for modern high-performance computing applications.

VI. BLOCK DIAGRAM

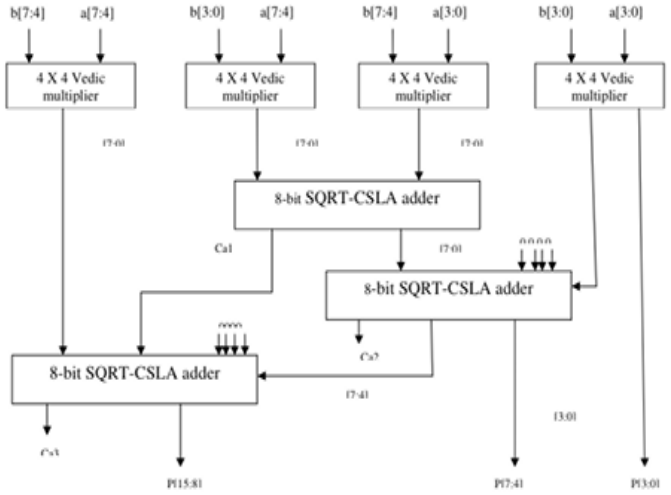

Fig. 6.2. Block Diagram

VII. RESULTS AND OUTCOMES

The proposed high-performance multiply–accumulate (MAC) unit was implemented and evaluated to analyze its effectiveness in terms of speed, area, and power consumption. The design was described using Verilog HDL and simulated under different input conditions to verify its functional correctness. Synthesis and performance evaluation were carried out using standard VLSI design tools, enabling a detailed comparison with conventional MAC architectures.

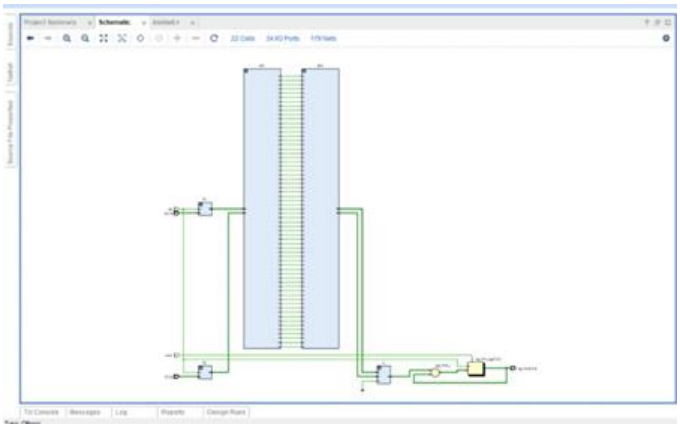

Fig: 7.1: Output 1

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The simulation results confirm that the proposed MAC unit operates correctly for all test cases, producing accurate multiplication and accumulation outputs. The waveform analysis demonstrates proper synchronization between partial product generation, reduction, and integrated accumulation stages. By embedding accumulation within the partial product reduction process, the design successfully eliminates redundant intermediate steps, resulting in a more streamlined data flow.

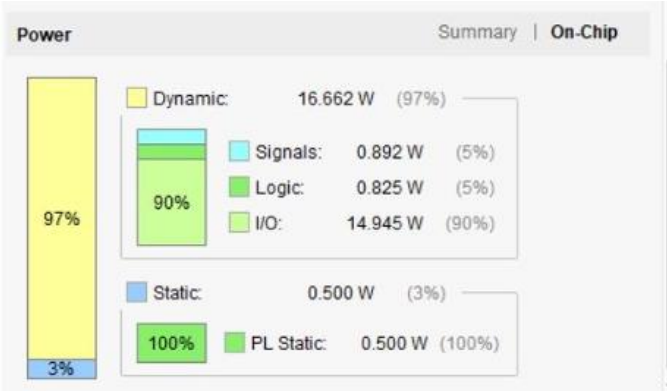

Fig:7.2: Output 2

One of the most significant outcomes of the proposed system is the reduction in critical path delay. Compared to traditional MAC units, which rely on separate multiplication and accumulation stages, the integrated approach shortens the computation path by minimizing carry propagation and reducing the number of sequential operations. As observed in the performance evaluation, delay improvements of more than 10–15% can be achieved depending on the word length, primarily due to the elimination of extra accumulation stages and optimized reduction techniques .

In terms of area utilization, the proposed design demonstrates a noticeable reduction in hardware complexity. By removing redundant correction terms and minimizing the number of adders required during partial product reduction, the overall gate count is reduced. This leads to more efficient silicon utilization, making the design suitable for compact VLSI implementations. The modular architecture also ensures scalability for larger bit-width designs without a proportional increase in complexity.

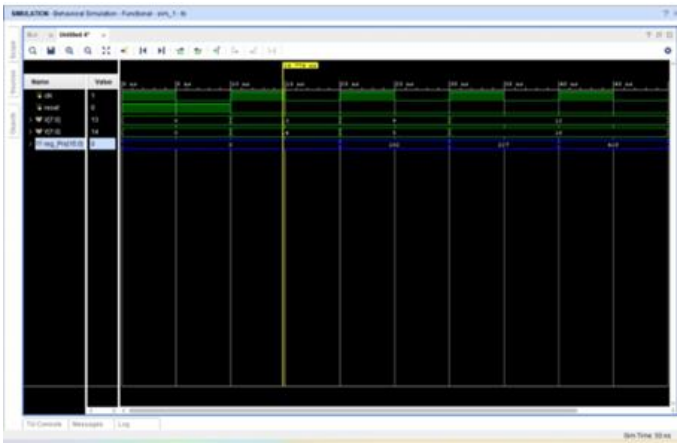

Fig: 7.3: Output 3

Power consumption is another important parameter considered in this work. The proposed MAC unit achieves lower power dissipation compared to conventional designs due to reduced switching activity and fewer logic transitions. The integration of operations decreases the number of active components during execution, thereby improving energy efficiency. This makes the architecture particularly beneficial for power-constrained applications such as embedded systems and portable devices.

Furthermore, the power-delay product (PDP), which represents the combined efficiency of speed and power, is significantly improved in the proposed system. The reduction in both delay and power consumption results in a lower PDP, indicating a more optimized and balanced design. This improvement becomes more pronounced for higher word-length operations, where traditional architectures tend to suffer from increased complexity and delay.

Overall, the results clearly demonstrate that the proposed MAC unit outperforms conventional architectures in terms of speed, area, and power efficiency. The integration of addition and accumulation into the partial product reduction process proves to be an effective strategy for enhancing performance. These outcomes validate the suitability of the proposed design for high-speed applications such as digital signal processing, image processing, and neural network acceleration, where efficient and rapid computation is essential.

VIII.CONCLUSION

In this work, a high-performance multiply–accumulate (MAC) unit has been successfully designed and implemented by integrating addition and accumulation operations into the partial product reduction process. The primary objective of reducing delay, power consumption, and hardware complexity has been effectively achieved through

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architectural optimization and efficient arithmetic techniques. Unlike conventional MAC units that treat multiplication and accumulation as separate sequential stages, the proposed design combines these operations into a unified computation flow, thereby eliminating redundant intermediate steps and improving overall efficiency.

The proposed architecture significantly reduces the critical path delay by minimizing carry propagation and decreasing the number of accumulation stages. By embedding accumulation within the partial product reduction tree, the design avoids the need for additional adders and intermediate storage elements. This leads to faster computation and improved throughput, making the system highly suitable for real-time applications. Furthermore, the use of optimized encoding and reduction techniques enhances the speed of multiplication while maintaining accuracy and reliability.

From a hardware perspective, the proposed MAC unit demonstrates improved area efficiency by reducing the number of logic gates and simplifying the overall structure. The elimination of unnecessary correction terms and redundant operations contributes to a more compact design, which is advantageous for VLSI implementations. In addition, the reduction in switching activity results in lower power consumption, making the design energy-efficient and suitable for portable and embedded systems.

The implementation using Verilog HDL and subsequent simulation and synthesis validate the correctness and effectiveness of the proposed approach. Performance evaluation shows that the design achieves better results in terms of delay, area, power consumption, and power-delay product compared to conventional MAC architectures. These improvements become more significant as the word length increases, highlighting the scalability of the proposed system.

Overall, the integration of addition and accumulation into the partial product reduction process provides a novel and efficient solution for high-speed arithmetic operations. The proposed MAC unit offers a balanced trade-off between performance, area, and power, making it an ideal candidate for advanced applications such as digital signal processing, image processing, and neural network accelerators. This work demonstrates that architectural innovation at the arithmetic level can lead to substantial improvements in system performance, paving the way for future research in optimized hardware design.

REFERENCES

1. Vellela, S. S., & Balamanigandan, R. (2024). Optimized clustering routing framework to maintain the optimal energy status in the wsn mobile cloud environment. Multimedia Tools and Applications, 83(3), 7919-7938.
2. Vellela, S. S., & Balamanigandan, R. (2023). An intelligent sleep-awake energy management system for wireless sensor network. Peer-to-Peer Networking and Applications, 16(6), 2714-2731.
3. Vellela, S. S., & Balamanigandan, R. (2024). An efficient attack detection and prevention approach for secure WSN mobile cloud environment. Soft Computing, 28(19), 11279-11293.
4. Vellela, S. S. (2023). Enhanced speckle noise reduction in breast cancer ultrasound imagery using a hybrid deep learning model. Ingénierie des Systèmes d'Information.
5. Polasi, P. K., Vellela, S. S., Narayana, J. L., Simon, J., Kapileswar, N., Prabu, R. T., & Rashed, A. N. Z. (2026). Data rates transmission, operation performance speed and figure of merit signature for various quadurature light sources under spectral and thermal effects. Journal of Optics, 55(1), 633-643.
6. Praveen, S. P., Nakka, R., Chokka, A., Thatha, V. N., Vellela, S. S., & Sirisha, U. (2023). A novel classification approach for grape leaf disease detection based on different attention deep learning techniques. International Journal of Advanced Computer Science and Applications (IJACSA), 14(6), 2023.
7. Vellela, S. S., Rao, M. V., Mantena, S. V., Reddy, M. J., Vatambeti, R., & Rahman, S. Z. (2024). Evaluation of Tennis Teaching Effect Using Optimized DL Model with Cloud Computing System. International Journal of Modern Education and Computer Science (IJMECS), 16(2), 16-28.
8. Vellela, S. S., & Krishna, A. M. (2020). On Board Artificial Intelligence With Service Aggregation for Edge Computing in Industrial Applications. Journal of Critical Reviews, 7(07).
9. Madhuri, A., Jyothi, V. E., Praveen, S. P., Sindhura, S., Srinivas, V. S., & Kumar, D. L. S. (2024). A new multi-level semi-supervised

Doi:10.48047/ijiee.2026.16.2.34

learning approach for network intrusion detection system based on the 'goa'. Journal of Interconnection Networks, 24(supp01), 2143047.
10. Raju, V. V. K., Bhavani, Y. V. K. D., Nandikonda, P., Kareemunnisa, F. N. U., Brahmeswara, K. B., & Sindhura, S. (2026). Iterative and Statistical Analytical Review of Predictive Modeling Approaches in Educational Systems: A Comprehensive Benchmark of AI-Driven Methods. International Journal of Innovative Technology and Interdisciplinary Sciences, 9(1), 490-522.
11. Biyyapu, N., Veerapaneni, E. J., Surapaneni, P. P., Vellela, S. S., & Vatambeti, R. (2024). Designing a modified feature aggregation model with hybrid sampling techniques for network intrusion detection. Cluster Computing, 27(5), 5913-5931.
12. Praveen, S. P., Vellela, S. S., & Balamanigandan, R. (2024). SmartIris ML: harnessing machine learning for enhanced multi-biometric authentication. Journal of Next Generation Technology (ISSN: 2583-021X), 4(1).
13. Vuyyuru, L. R., Purimetla, N. R., Reddy, K. Y., Vellela, S. S., Basha, S. K., & Vatambeti, R. (2025). Advancing automated street crime detection: a drone-based system integrating CNN models and enhanced feature selection techniques. International Journal of Machine Learning and Cybernetics, 16(2), 959-981.
14. Vellela, S. S., Roja, D., Purimetla, N. R., Thalakola, S., Vuyyuru, L. R., & Vatambeti, R. (2025). Cyber threat detection in industry 4.0: Leveraging GloVe and self-attention mechanisms in BiLSTM for enhanced intrusion detection. Computers and Electrical Engineering, 124, 110368.
15. Vellela, S. S., Pushpalatha, D., Sarathkumar, G., Kavitha, C. H., & Harshithkumar, D. (2023). Advanced intelligence health insurance cost prediction using random forest. ZKG International, 8.
16. Vellela, S. S., Babu, B. V., & Mahendra, Y. B. (2024). IoT-based tank water monitoring systems: enhancing efficiency and sustainability. International Journal for Modern Trends in Science and Technology, 10(02), 291-298.
17. Vellela, S. S., Varshini, K., Jeevana, M., Kadheer, S. K., & Kumar, T. P. (2024). Iot based smart irrigation and controlling system. IoT Based Smart Irrigation and Controlling System, International Journal for Modern Trends in Science and Technology, 10(02), 77-85.
18. Vellela, S. S., Chaganti, A., Gadde, S., Bachina, P., & Karre, R. (2022). A Novel Approach for Detecting Automated Spammers in Twitter. Mukt Shabd, 11, 49-53.
19. Vellela, S. S., Narapasetty, S., Somepalli, M., Merikapudi, V., & Pathuri, S. (2022). Fake News Articles Classifying Using Natural Language Processing to Identify in-article Attribution as a Supervised Learning Estimator. Mukt Shabd Journal, 11.
20. Vellela, S. S., Vineeth, S., & Suresh, V. (2024). IoT Based ICU Patient Monitoring System. IoT Based ICU Patient Monitoring System, International Journal for Modern Trends in Science and Technology, 10(02), 265-273.
21. Vellela, S. S., & Balamanigandan, R. (2025). Designing a Dynamic News App Using Python. Available at SSRN 5250912.
22. Vellela, S. S., Rao, M. V., Krishna, C. V. M., Rao, T. S., & Dasthavejula, R. (2026). Piezoelectric and Shape-Memory Materials for Actuators and Energy Harvesting in Mechanical, Electronics, and Biomedical Engineering Using AI-Based Design. In Advanced Materials for Biomedical Devices (pp. 195-206). CRC Press.
23. Vellela, S. S., Singu, K., Kakarla, L. S., Tadikonda, P., & Sattenapalli, S. N. R. (2025). NLP-Driven Summarization: Efficient Extraction of Key Information from Legal and Financial Documents. Available at SSRN 5250908.
24. Vellela, S. S., Anusha, P., Vullam, N. R., Jala, J., Bellapu, V. S., & Vindhya, A. S. (2025, October). Quantum Cryptography and Key Distribution for Secure Communication in the Post Quantum World. In 2025 International

Doi:10.48047/ijiee.2026.16.2.34

Conference on Sustainable Communication Networks and Application (ICSCN) (pp. 619-624). IEEE.
25. Roja, D., Jidugu, S. K., Rao, T. S., Vuyyuru, L. R., Vellela, S. S., & Ranjani, B. S. (2025, December). High-Fidelity Image Synthesis using Enhanced Generative Adversarial Networks with Attention Mechanisms. In 2025 International Conference on NexGen Networks and Cybernetics (IC2NC) (pp. 885-890). IEEE.
26. Vellela, S. S., Vuyyuru, L. R., Jidugu, S. K., Rao, M. P., & Srinivas, B. R. (2025, November). The Impact Of Quantum Computing On Blockchain Security And Quantum Resistant Protocols. In 2025 2nd International Conference on Intelligent Systems for Cybersecurity (ISCS) (pp. 1-6). IEEE.
27. Yanamadala, N., & Vellela, S. S. (2025, June). Ensuring Authenticity and Confidentiality in Images using SHA-ECC Fusion. In 2025 Second International Conference on Networks and Soft Computing (ICNSoC) (pp. 684-689). IEEE.
28. Vellela, S. S. (2024). A Comprehensive Review of AI Techniques in Serious Games: Decision Making and Machine Learning.
29. Burra, R. S., APCV, G. R., & Vellela, S. S. (2024). Strategic Insights: Unleashing the Power of Big Data Analytics for Credit Investigation and Risk Mitigation in Commercial Banking. International Journal of Progressive Research in Engineering Management and Science, 4(01), 458-464.
30. Vellela, S. S., Purimetla, N. R., Vindhya, A. S., Vullam, N. R., Srinivas, B. R., & Vuyyuru, L. R. (2025, October). Design and Simulation of Quantum Error Correction Codes for Scalable Quantum Architectures. In 2025 7th International Conference on Innovative Data Communication Technologies and Application (ICIDCA) (pp. 1570-1575). IEEE.
31. Vellela, S. S., Purimetla, N. R., Rao, P. V., Daniel, V. A. A., Koppolu, H. K. R., & Janani, B. (2025). AI-Enabled Wearable Hemodynamic Monitoring System for Early Identification of Thrombotic Events. Vascular and Endovascular Review, 8(16s), 321-336.
32. Venkatesh, N., Maheswari, S., & Triveni, P. (2024). Harnessing IoT for Real-Time Plant Health Monitoring: Challenges and Opportunities.
33. Reddy, B. V., Kumar, A. H., Gopi, C., Prasad, Y. V. D., Vellela, S. S., & Roja, D. (2025, April). Machine learning based automated liver fibrosis stage diagnosis with prediction. In 2025 International Conference on Advances in Modern Age Technologies for Health and Engineering Science (AMATHE) (pp. 1-6). IEEE.
34. Rao, M. V., Sreeraman, Y., Mantena, S. V., Gundu, V., Roja, D., & Vatambeti, R. (2024). Brinjal Crop yield prediction using Shuffled shepherd optimization algorithm based ACNN-OBDLSTM model in Smart Agriculture. Journal of Integrated Science and Technology, 12(1), 710-710.
35. Haritha, K., Geethika, N. S., Venkateswarlu, K., Kumar, R. H., & Ramakrishna, Y. Enhancing Public Safety with AI & ML-Based CCTV Surveillance.
36. Haritha, K., Prakash, P. B., Pravallika, D., Venkatesh, K., & Venkatesh, G. Enhancing Object Detection in Autonomous Vehicles Under Low-Light Conditions Using Federated Learning and YOLOv5.
37. Ram, C. S., Vellela, S. S., Sravanthi Javvadi, D. V., Rashid, S. Z., & Madhumathi, S. M. (2025). Integrated Robotic–Imaging Platforms in Endovascular Surgery: Current Capabilities and Future Directions. Vascular and Endovascular Review, 8(16s), 285-298.
38. Roja, D., Navya, G., Srujana, B. S., Mamatha, P., & Sai, C. Y. K. Deep Learning for Hotel Reviews: A Framework for Sentiment Classification and Fake Review Detection.
39. Pakalapati, S., Rani, C. J., Vellela, S. S., Thanuja, N., & Bindu, M. N. H. (2025, November). Progressive GAN-based Framework for Realistic Image Generation and Style Transfer. In 2025 5th International Conference on Evolutionary Computing and Mobile Sustainable Networks (ICECMSN) (pp. 474-479). IEEE.

Doi:10.48047/ijiee.2026.16.2.34

40. Balamanigandan, R., Vellela, S. S., Gorintla, S., Vuyyuru, L. R., Thanuja, N., & Rao, T. S. (2025, September). Quantum-Enhanced Data Security for Electronic Health Records: A Framework for Post-Quantum Cryptography in Healthcare Systems. In 2025 6th International Conference on Smart Electronics and Communication (ICOSEC) (pp. 1924-1929). IEEE.
41. Roja, D., Amulya, P., Nagasai, M., Prasad, D. D., & Babu, A. V. Machine Learning-Based Early Diagnosis of Fish Diseases via Water Quality Data.
42. Sai, M. B., & Vellela, S. S. (2025, December). Hybrid ML Driven Multi-Cloud Service Work Load Prediction For Financial Systems. In 2025 1st International Conference on Advancement in Futuristic Technologies (ICAFT) (pp. 1-6). IEEE.
43. Kareemunnisa, D., Haritha, K., Ranjani, B. S., Venkateswarlu, K., & Bindu, M. N. H. DUAL-STAGE PRIVACY PROTECTION FOR GRAPH NEURAL NETWORKS AGAINST INFERENCE ATTACKS.
44. Mandava, R., Haritha, K., Vellela, S. S., Purimetla, N. R., Mohan, B. K., & Harinadh, T. (2025, June). Analysing User Perceptions of Trust in Financial Systems Using Explainable AI. In 2025 Second International Conference on Networks and Soft Computing (ICNSoC) (pp. 26-30). IEEE.

Doi:10.48047/ijiee.2026.16.2.34