Performance-Driven Design and Evaluation of Dynamic Comparators in Low-Power SAR ADCs

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Abstract: This paper presents a comprehensive analysis and classification of comparators used in low-power and low-data-rate Successive Approximation Register Analog-to-Digital Converters (SAR ADCs). Both voltage-domain and time-domain comparator architectures are investigated with respect to power consumption, comparison speed, noise performance, and kickback effects. Several widely adopted dynamic voltage-domain comparators are studied in detail to evaluate their suitability for low-voltage SAR ADC applications. The analysis reveals that impedance asymmetry in the DAC switching network introduces significant differential kickback noise, which adversely affects comparator accuracy, especially during least significant bit (LSB) conversion stages. To overcome these limitations, a modified comparator architecture incorporating a pre-amplifier stage is proposed. The pre-amplifier improves the input signal strength prior to regeneration, thereby reducing kickback noise, minimizing input-referred offset, and enhancing overall noise immunity under low supply voltage conditions. In addition, digitally assisted offset compensation techniques are analysed to determine the minimum tuning requirements for improved accuracy. Design trade-offs among power consumption, noise performance, DAC loading, and comparison speed are systematically evaluated. The proposed comparator architecture is implemented and simulated using 130 nm CMOS technology in Tanner EDA tools. Simulation results demonstrate improved accuracy, robustness, and reliable low-power operation, making the proposed design highly suitable for energy-efficient SAR ADC applications.

Key Words: Dynamic Comparator, SAR ADC, Low-Power Design, CMOS Technology, Propagation Delay, Noise Performance, Regenerative Latch, VLSI Design.

1.Introduction

Successive Approximation Register (SAR) Analog-to-Digital Converters (ADCs) are widely used in low-power and medium-resolution applications due to their simple architecture, high energy efficiency, and scalability. SAR ADCs are extensively utilized in biomedical instruments, wireless sensor networks, industrial monitoring systems, portable electronic devices, and Internet of Things (IoT) applications, where low power consumption and compact silicon area are essential design requirements. Among the key building blocks of a SAR ADC, the comparator plays a critical role in determining the converter's accuracy, conversion speed, linearity, and overall power efficiency. As CMOS technology continues to scale toward lower supply voltages and deep-

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submicron processes, the design of high-speed and low-power comparators has become increasingly challenging due to reduced voltage headroom, device mismatch, and noise sensitivity.

Dynamic voltage-domain comparators are widely preferred in low-power SAR ADC architectures because they consume nearly zero static power and provide fast regenerative operation. Comparator architectures such as Strong ARM latch and double-tail dynamic comparators are commonly used owing to their high-speed performance and reduced power dissipation. However, low-voltage operation introduces several non-ideal effects including increased input-referred offset, regeneration delay, kickback noise, and reduced common-mode input range. Among these challenges, clock kickback noise significantly affects comparator accuracy by coupling switching transients from internal nodes back to the input terminals through parasitic capacitances. In practical SAR ADC implementations, asymmetry in the capacitive DAC network caused by unequal switch resistances and layout parasitics converts common-mode kickback into differential kickback noise, which severely impacts least significant bit (LSB) decision accuracy and overall ADC linearity.

To overcome these limitations, advanced comparator architectures and compensation techniques have been proposed for low-voltage high-speed ADC applications. Techniques such as body-driven transistors, supply boosting, bootstrapping, and double-tail structures improve comparator operation under reduced supply voltages; however, they often introduce additional complexity, reliability concerns, or increased power consumption. In this work, a modified comparator architecture incorporating a pre-amplifier stage is proposed to improve noise immunity, reduce input-referred offset, and minimize kickback noise. The pre-amplifier enhances the input signal before regeneration, enabling reliable operation at low supply voltages while maintaining acceptable power consumption. Furthermore, the design trade-offs among power dissipation, noise performance, kickback suppression, and DAC loading are systematically analysed using 130 nm CMOS technology in Tanner EDA tools. The proposed architecture demonstrates improved accuracy, robustness, and energy efficiency, making it highly suitable for low-power SAR ADC applications.

2.Literature Survey

H. S. Bindra, C. E. Lokin, D. Schinkel, A.-J. Annema, and B. Nauta proposed a low-noise dynamic bias latch-type comparator implemented in 65-nm CMOS technology. The design incorporates a dynamic bias pre-amplifier with a tail capacitor to minimize energy consumption while maintaining low input-referred noise. The pre-amplifier ensures partial discharge of output nodes, thereby reducing switching power and improving efficiency. The authors also presented analytical optimization methods for achieving high gain and low noise performance. Experimental results demonstrated significant reduction in energy consumption with improved comparator sensitivity, making the architecture suitable for low-power high-speed ADC applications.

Y. T. Wang et al. presented an 8-bit high-speed pipelined and interleaved CMOS Analog-to-Digital Converter (ADC) designed for high conversion rates using open-loop analog processing circuits. The

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proposed architecture employed techniques such as sliding interpolation, distributed sampling, and clock edge reassignment to improve speed and reduce timing mismatches and nonlinearity errors. The design minimized the requirement for complex residue amplifiers and large comparator arrays, thereby reducing hardware complexity. Implemented using 0.6-µm CMOS technology, the converter achieved improved linearity and high sampling performance, demonstrating its effectiveness for high-speed data conversion applications.

3.Existing System

Existing comparator architectures generally employ open-loop comparators or regenerative latch comparators for analog-to-digital conversion applications. Open-loop comparators are based on operational amplifiers without feedback and suffer from high delay, low accuracy, and increased power consumption, making them unsuitable for high-speed and low-power applications. To overcome these limitations, dynamic latch comparators are widely adopted due to their faster operation and zero static power dissipation. The conventional dynamic latch comparator consists of an input pre-amplifier stage followed by a regenerative latch stage. During the reset phase (CLK = 0), the output nodes are pre-charged to logic high. In the amplification phase (CLK = 1), the differential input signal is amplified and transferred to the latch stage. Finally, during the regeneration phase, the latch rapidly drives the outputs to either VDD or ground through positive feedback action. Although this structure improves speed and power efficiency, it suffers from limitations such as kickback noise, offset voltage, limited input range, and reduced performance at low supply voltages due to the use of pMOS input pairs in the latch stage.

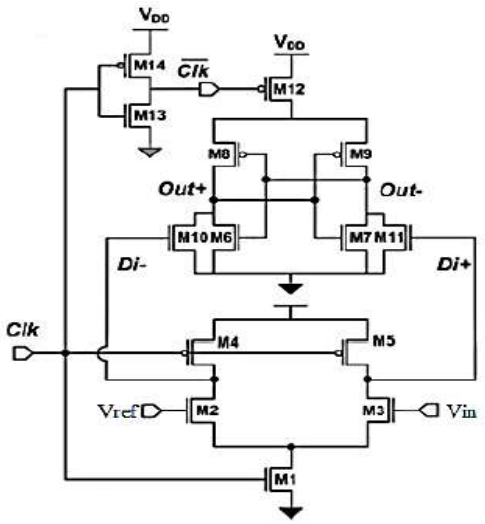

Fig 3.1: Circuit diagram of Conventional Double-tail Dynamic latch comparator

The conventional SAR ADC system uses a dynamic double-tail latch comparator for high-speed and low-power analog-to-digital conversion. The comparator consists of separate input and latch stages, enabling efficient operation at low supply voltages with improved speed and reduced power consumption. During the reset phase, internal nodes are pre charged to a known voltage level, while during the evaluation phase, the differential input voltage from the DAC is amplified through regenerative positive feedback to generate a digital output. The double-tail structure allows independent current control for the input and latch stages, resulting in faster decision making and better stability compared with single-tail comparators. The existing dynamic comparator architecture suffers from kickback noise, offset voltage, and reduced noise immunity, which degrade the accuracy of SAR ADC performance. Impedance mismatch and parasitic effects in the DAC introduce differential kickback noise, particularly during LSB conversion at low supply voltages. These limitations

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increase propagation delay, reduce conversion accuracy, and affect the overall efficiency of low-power SAR ADC systems.

4.Proposed System

The proposed system introduces an optimized dynamic comparator architecture for low-power and low-data-rate SAR ADC applications using 130 nm CMOS technology. The design focuses on reducing kickback noise, offset voltage, and power consumption while improving conversion accuracy and operating reliability. A voltage-domain comparator with an improved preamplifier-latch structure is employed to achieve stable operation under reduced supply voltages. The architecture uses a symmetric clock distribution network and balanced input layout to minimize impedance mismatch and differential kickback noise from the DAC.

During operation, the comparator performs reset and evaluation phases to generate accurate digital decisions with regenerative positive feedback. A controlled slew-rate clock buffer is incorporated to suppress high-frequency charge injection and reduce clock kickback noise. The proposed design also integrates a digitally assisted offset calibration mechanism using a binary-weighted capacitor array to compensate mismatch-induced offset errors. Simulation results demonstrate reduced kickback noise, lower offset voltage, faster comparison speed, and improved energy efficiency compared with conventional comparator architectures. Owing to its low-power operation and enhanced accuracy, the proposed system is highly suitable for biomedical devices, IoT sensor interfaces, and portable SAR ADC applications.

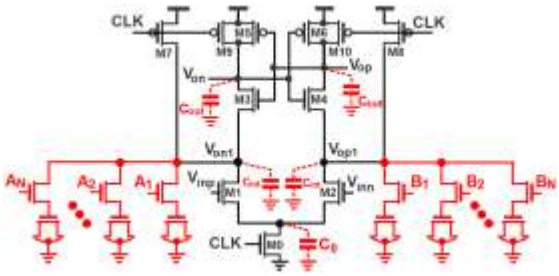

Fig 4.1: Comparator with tuned capacitor Array.

The proposed SAR ADC comparator architecture consists of a pre-amplifier stage followed by a dynamic latch stage. The pre-amplifier amplifies the small differential input signal from the DAC and isolates the input from latch switching disturbances, thereby reducing kickback noise and offset effects. During the reset phase, internal nodes are pre charged, while in the evaluation phase the amplified signal is applied to the latch, where regenerative positive feedback produces the final digital output. A symmetric layout, balanced DAC switching network, and controlled slew-rate clock buffer are incorporated to suppress differential kickback noise and improve low-voltage operation.

4.1Methodology

The proposed methodology presents a low-power, high-speed dynamic comparator for SAR ADCs by combining kickback noise reduction, offset calibration, and energy-efficient design techniques. A modified comparator architecture based on strong-arm and double-tail comparators is employed to minimize differential kickback noise through balanced input impedance and symmetrical routing. An optimized pre-amplifier enhances sensitivity and reduces input-referred noise, improving decision accuracy under low-voltage conditions. To reduce power consumption, a dynamic clock-controlled switching mechanism activates the comparator only during comparison operations. Additionally, a

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digitally assisted offset calibration scheme compensates for process variations and transistor mismatches, ensuring reliable and accurate conversion. The design is implemented and evaluated using CMOS technology, demonstrating improved conversion accuracy, lower power consumption, faster DAC settling, and reduced offset voltage, making it suitable for 8–12-bit SAR ADC applications in biomedical, IoT, and portable electronic systems.

5.Results and Discussion

The study shows that dynamic comparators strongly influence the speed and power efficiency of SAR ADCs. Among all architectures, the double-tail dynamic comparator achieved the best performance for low-power and high-speed applications.

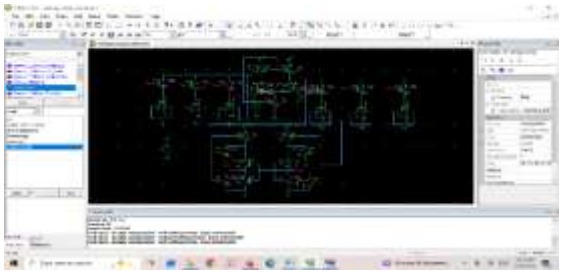

Fig 5.1: Proposed Circuit Diagram

The fig 5.1 shows a dynamic comparator using a differential input pair and latch stage to enable fast decision-making with low power consumption in SAR ADCs.

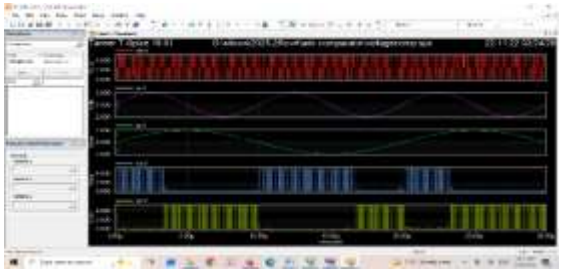

Fig 5.2: Simulation Waveform

Fig. 5.2 shows the comparator waveform with proper switching and confirms fast, stable operation.

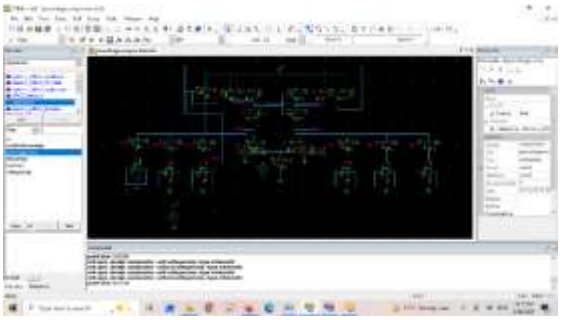

Fig 5.3: Extension Circuit Diagram

Fig.5.3 shows the circuit diagram of the proposed dynamic comparator for the SAR ADC. The proposed design is optimized to achieve lower power consumption, reduced delay, and improved comparison speed. It also enhances overall ADC performance with efficient switching operation.

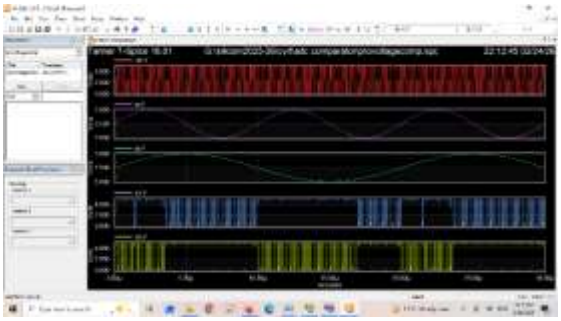

Fig 5.4: Simulation Waveform

Fig 5.4 shows the proposed comparator waveform, indicating faster switching, stable output, and improved low-power high-speed performance.

	Existing System	Proposed System
Area	27	23
Power	1.576×10^{-5}	2.58×10^{-5}

Table1: Compression Table

The comparison shows that the proposed design achieves better area efficiency with a more compact implementation. Although there is a slight increase in power consumption, it still maintains acceptable performance for SAR ADC applications.

6.Conclusion and Future Scope

The study presents a comprehensive evaluation of comparator architectures for low-power SAR ADCs and identifies

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differential clock kickback, offset voltage, and noise sensitivity as major performance-limiting factors in conventional designs. A pre-amplifier-based comparator is proposed to mitigate these issues by isolating input nodes from latch switching disturbances and improving signal strength before regeneration. Simulation results in 130 nm CMOS technology confirm that the proposed architecture significantly enhances accuracy, noise immunity, and overall conversion reliability under low-voltage operation. Although there is a minor increase in power and complexity, the trade-off is justified by the substantial improvement in performance, making the design suitable for modern low-power applications.

Future Scope: Future work can focus on further reducing power consumption using advanced subthreshold and near-threshold design techniques. The architecture can also be extended to higher-resolution SAR ADCs with improved calibration schemes and implemented in more advanced CMOS technologies for better speed and energy efficiency.

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