Semiconductor Die: Processing and Packaging

Satya Sai Srikant and Rajendra Prasad Mahapatra

***Abstract*—This paper presents the processes, steps and inspections, various testing stages involved starting from procurement of wafer onwards to individual Die form. Any semiconductor die or integrated circuit must performed all the processes of inspection and testing once it receives from any manufacturer and then it has to be procured to any Manufacturing Line for further process as a part of any Manufacturing products. This paper is also an attempt to isolate the entire good and bad Semiconductor Dies received from some Semiconductor Manufacturer at one place with complete package before going to Manufacturing Unit. It not only yields the efficiency of the Product in that Manufacturing line but also it saves a lot of manpower given for Failure Analysis, rework, retesting, etc and also it increases the Product reliability**

***Index Terms*—Resonance, wafer, die, lapping, voids**

I. Introduction

Any small change in the product which may be either due to process improvement or due to application requirements or due to material changes had a direct impact on device reliability. The device reliability depends upon avoiding any small and minute changes from the original one. For example any changes in die size which occurred due to scratch, die track cut, chips out, cracks, voids, corrosion on bond pads, glassivation, metallization, passivation, leads to decrement of Product performance.

For an instant, the capacitor of cracked Die [1] becomes either half for parallel circuited or get doubled for series circuited. In both the cases, the resonance for the Product affects and hence the performance degrades. If there are any voids or corrosion on bond pads, the series inductance increases which again degrades. Hence for successful Product launching; the associated items should be understood about their functionality, performance and also to be prevented to avoid any type of changes in size and shape.

II. Basics

The Semiconductor Die or chip is the heart of any electronic products. This small Die contains a lot of integrated circuits and full of intelligence associated with it. The Die may be designed according to a design methodology that includes the step of concurrently designing circuitry and a product circuitry in a unified design. This Paper will discuss complete processes for Die processing and packaging much prior allocating to Manufacturing Unit.

Manuscript received on January 30, 2011; revised April 25,2012. This work is based on the Die and ICs received by different semiconductor manufacturers. These Dies and ICs should be done proper processed and packaging before going to production unit.

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III. Wafer's Inspection

A. Wafer Inspections

The Semiconductor Die from Manufacturer comes in a Wafer package of size with minimum 6 inch Diameter with thickness 15-20 mils. It is as shown in Fig. 1. This Wafer package has to be done a Visual Inspection (VI) with magnifying microscope with a magnification of 60 X – 100 X. It has to be checked whether there is any glassivation or passivation or metallization shown in Fig. 2. Also Die has to be inspected constantly whether there is any presence of Voids Fig. 3 corrosion in Bond Pad Fig. 4 or any Die crack Fig. 5 or any contamination [2],[3] on Die Surfaces. The VI Reports should be recorded and submitted along with the wafers.

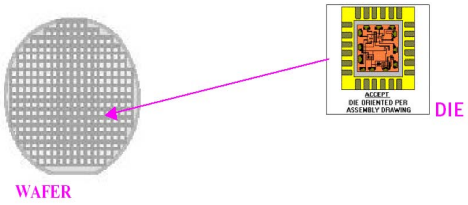


Fig. 1. Semiconductor die in wafer

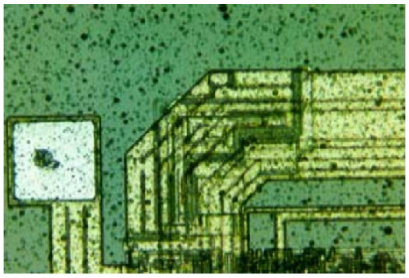


Fig. 2. Passivations, glassivations and metallization

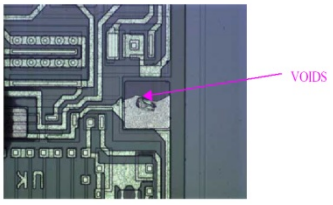


Fig. 3. Voids in glassivation

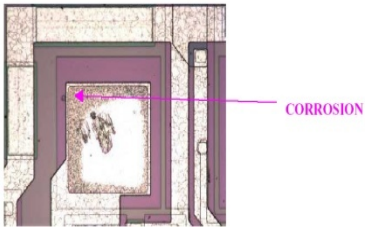


Fig. 4. Corrosion in bond pads

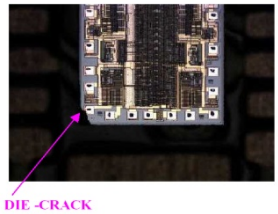


Fig. 5. Cracks in die

B. Electrical Testings

The next process for all the Bare Die in Wafer is Electrical testing i.e. DC – probe Testing [3], [4]. In this testing, a single Bare Die is placed on the Probe Card. The automatic tester shown in Fig. 6 will give the proper signal if it gives desired signal indication for Bare Die connected via Probe needles [4] to tester. This test can also be performed directly on wafer also for each Die.

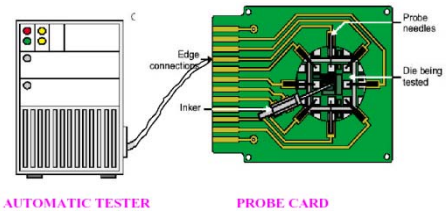


Fig. 6. DC – probe testing set

If the tester does not give any signal or less than the desired signal then the Bare Die is inked as shown in Fig. 7 indicating as a Bad Die. No signal for a Bare Die clearly indicates that there must be track cut or corrosion on Die. Also low signal indicates that there must be some crack or voids or metallization on Bare Die due to which the Capacitive value either decreases or increases which affects the resonant factor directly.

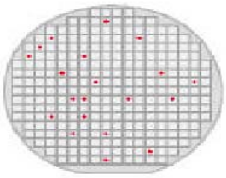


Fig. 7. Bad dies inked

Once the process of Bad Dies Inked for the Wafer completed with Electrical Testing, then the yield or efficiency for good Die should be calculated. The standard for Wafer acceptance and rejection criteria should always be followed as testing standard.

C. Visual Inspections

There should be a process of Visual Inspection again, soon after Electrical Testing process. Under this process, VI with high magnifying Microscope (60 X – 100 X) is required for excessive probe impression and scratches. Fig. 8 shows a Die with excessive probe impression and scratches during electrical testing. The Die with such impression and scratches must keep in separate Wafer even though functionality wise is good. The yield or efficiency for good Die in original Wafer and also the yield to be calculated for good Die with excessive probe impression which with in separate Wafer. The VI report for both Good and probe impression Bare Die should be recorded in a detailed way.

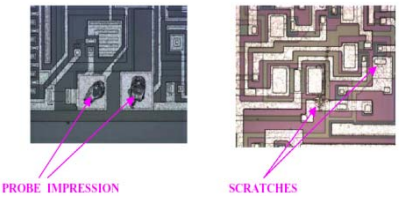


Fig. 8. Probe impression and scratches on die

D. Packing the Good Wafers

After the Visual Inspection process, all the Good Wafers [5] should pack in free contamination Wafer Casing, shown in Fig. 9.

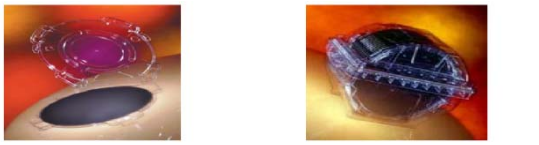


Fig. 9. Casing with single wafer and multiple wafers

IV. Lapping and Polishing

A. Lapping and Polishing

The procedure for Lapping process shall be compatible with Semiconductor wafers [5].

a) Wafer must be reduced to 175mm ± 5mm thickness
b) After lapping process, it should be cleaned by suitable solvent.
c) Measure and record thickness of Lapping (as per desired specifications only) at 4-5 places for the wafer. The thickness should be constant and it always be as per specifications.

B. Visual Inspection

A process of Visual Inspection is again there soon after Lapping / polishing process. The VI with high magnifying Microscope (60 X – 100 X) is required for VI for any voids and scratches; VI for damaging to glassivations. It is shown in Fig. 10 which occurs during Lapping / polishing process. The yield or efficiency for good Lapped Die should be calculated and recorded.

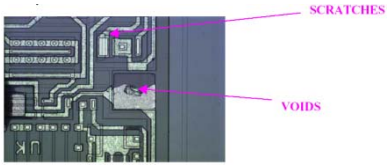


Fig. 10. Voids and scratches after lapping process

C. Mounting the Wafer

Fig. 11. Glue tapping

The next process is to mount the Wafer with Glue Tape and Bracket as shown in Fig. 11. It should be always crossed check that there should not be any voids on Glue Tape. A process of thorough VI to be performed with high microscope (60X – 100X) to check whether the proper mounting of wafer

has been performed and also to avoid any voids on Glue tapes and Brackets.

D. Dicing and Cleaning

After all the above processes, the most important step is to dice the wafer as per the drawing provided from the Design Department. The diced wafer is shown in Figure (12). The cleaning process of wafer should be performed after dicing and then observe the VI for defects if any.

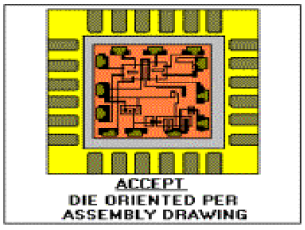
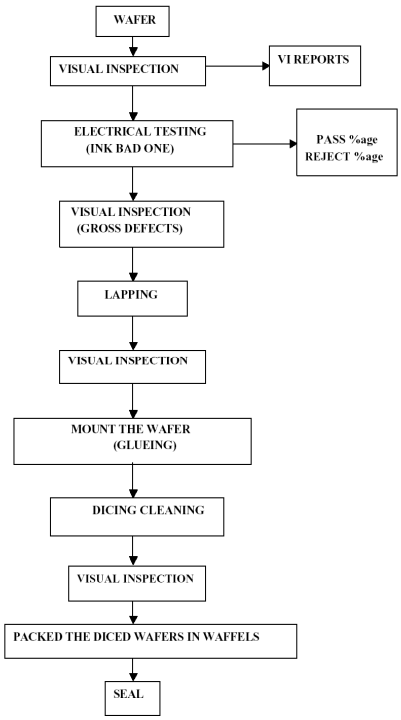


Fig. 12. Diced wafer

TABLE I PROCESS FLOW DIAGRAM



V. PROCESS FLOW DIAGRAM

The process flow diagram of entire processes from procurement of wafer to individual diced Die is shown in Table 1. The experiment is performed for the IC named T-5557e from ATMEL [6].

VI. CONCLUSION

This paper presents a competitive process of testing and inspection, involved from procurement of wafer to diced individual Die. On adopting the above process, the selection of any semiconductor ICs for any manufacturing the product shows excellent success rate with almost zero failure result. The integrated circuit T 5557e from ATMEL with above process has been experimented for the production of Smart Card and Smart Card Reader. The integrated circuit is used in the Die form and is lapped and polished to a thickness of 175 mm.

ACKNOWLEDGMENT

There are far too many people to try to thank them all many people have contributed to the development of this paper. We owe our deep regards and honor to express our gratitude to Dr. Manoj Kumar Pandey, Director, SRM-Institute of Management & Technology, Modinagar and all the faculty members for providing me invaluable support, guidance, help and inspiration all through this paper.

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