

Bandgap Reference Layout Analysis and Design

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Abstract—Analog circuits incorporate voltage and current reference extensively. Such references are dc quantities that exhibit little dependence on supply and process parameters and a well-defined dependence on the temperature. In systems such as A/D and D/A converters and so on, a reference is required to define the input and output full-scale range. In this paper, the analysis and layout design of reference generator in CMOS technology are dealt with, being focused on well-establishing “bandgap” technique. First, supply-independent biasing is studied. Next, temperature-independent references are described and issues such as the effect voltage are examined. Third, bandgap reference layouts are designed and the results are given. Finally, an example of state-of-the-art bandgap references are studied.

Index Terms—Bandgap, layout, supply-independence, temperature-independence, mismatch, matching.

I. INTRODUCTION

The objective of reference generation is to establish a dc voltage or current that is independence of the supply and process and has a well-defined behavior with temperature. In most applications, the required temperature dependence assumes one of three forms: (a) proportional to absolute temperature (PTAT); (b) Constant- G_m behavior. i.e., such that the transconductance of certain transistor remains constant; (c) temperature independent. Therefor the task is divided into two design problems: supply-independence biasing and definition of the temperature variation.

II. SUPPLY-INDEPENDENT BIASING

The use of bias current and current mirrors has implicitly assumed that a “golden” reference current is available. As shown in Fig. 1(a) and (b), if I_{REF} does not vary with V_{DD} and channel-length modulation of M2 and M3 is neglected, then I_{OUT} remains independent of the supply voltage.

In order to arrive at a less sensitive solution, the circuit must bias itself, i.e., I_{REF} must be somehow derived from I_{OUT} . Fig. 1 illustrates an implementation where M3 and M4 copy I_{out} , thereby defining I_{REF} . Since I_{out} and I_{REF} in Fig. 1 are relatively independent on V_{DD} . If M1-M4 operate in saturation $\lambda \approx 0$ where λ is the channel-length modulation coefficient, then the circuit is governed by only one equation, $I_{out} = KI_{REF}$, and hence can support any current level! To uniquely define the current, resistor R_S decreases the current of M2 while the PMOS devices require that $I_{out} = I_{REF}$ because they have identical dimensions. $V_{GS1} = V_{GS2} + I_{D2}R_S$

can be written, or

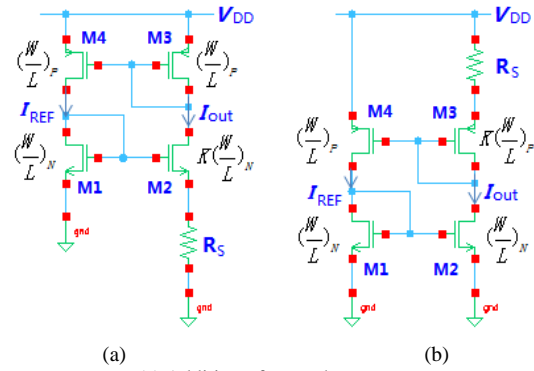
$$\sqrt{\frac{2I_{out}}{\mu_n C_{ox}(W/L)_N}} + V_{TH1} = \sqrt{\frac{2I_{out}}{\mu_n C_{ox}K(W/L)_N}} + V_{TH2} + I_{out}R_S \quad (1)$$

Neglecting body effect, we have

$$\sqrt{\frac{2I_{out}}{\mu_n C_{ox}(W/L)_N}} \left(1 - \frac{1}{\sqrt{K}}\right) = I_{out}R_S \quad (2)$$

And hence

$$I_{out} = \frac{2}{\mu_n C_{ox}(W/L)_N} \left(\frac{1}{R_S^2} \left(1 - \frac{1}{\sqrt{K}}\right)\right) \quad (3)$$



(a) Addition of R_S to the currents
(b) Alternative implementation eliminating body effect
Fig. 1. Establishing Supply-Independent Current using R_S .

The assumption $V_{TH1} = V_{TH2}$ introduces some errors in the foregoing calculations because the sources of M1 and M2 are at different voltage. Shown in Fig. 1(b), a simple remedy is to place the resistor in the source of M3 while eliminating body effect by tying the source and bulk of each PMOS transistor. The circuit of Fig. 1(a) and (b) exhibit little supply dependence if channel-length modulation is negligible. For this reason, relatively long channels are used for all of the transistors in the circuit.

III. TEMPERATURE-INDEPENDENT REFERENCE

Reference voltage or currents that exhibit little dependence on temperature prove essential in many analog circuits. It is interesting to note that, since most process parameters vary with temperature, if a reference is temperature-independent, then it is usually process-independent as well.

A. Negative-TC (Temperature Coefficient) Voltage

The base-emitter voltage of bipolar transistors or, more generally, the forward voltage of a PN-junction diode exhibits a negative.

For a bipolar device we have $I_C = I_S \exp(V_{BE} / V_T)$, where $V_T = \kappa T / q$. The saturation current I_S is proportional to $\mu \kappa T n_i^2$, where μ denotes the mobility of minority carriers, κ is Boltzmann constant and n_i is the intrinsic minority carrier concentration of silicon.

$$I_S = b T^{4+m} \exp \frac{-E_g}{\kappa T} \quad (4)$$

where b is a proportionally factor, $E_g \approx 1.12 \text{ eV}$ is the bandgap energy of silicon and $m \approx 3/2$. Writing $V_{BE} = V_T \ln \frac{I_C}{I_S}$, we can compute the TC of the base-emitter voltage as follow.

$$\frac{\partial V_{BE}}{\partial T} = \frac{\partial V_T}{\partial T} \ln \frac{I_C}{I_S} - \frac{V_T}{I_S} \frac{\partial I_S}{\partial T} \quad (5)$$

From (4), the equation (6) is obtained.

$$\frac{\partial I_S}{\partial T} = b(4+m)T^{3+m} \exp \frac{-E_g}{\kappa T} + bT^{4+m} \left(\exp \frac{-E_g}{\kappa T} \right) \left(\frac{E_g}{\kappa T^2} \right) \quad (6)$$

Therefore,

$$\frac{V_T}{I_S} \frac{\partial I_S}{\partial T} = (4+m) \frac{V_T}{T} + \frac{E_g}{\kappa T^2} V_T \quad (7)$$

With the aid of (5) and (7), the equation (8) and (9) are obtained.

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_T}{T} \ln \frac{I_C}{I_S} - (4+m) \frac{V_T}{T} - \frac{E_g}{\kappa T^2} V_T \quad (8)$$

$$= \frac{V_{BE} - (4+m)V_T - E_g / q}{T} \quad (9)$$

The equation (9) gives the temperature coefficient of the base-emitter voltage at a given temperature T , revealing dependence on the magnitude of V_{BE} itself. With $V_{BE} \approx 750 \text{ mV}$ and $T = 300 \text{ K}$, $\partial V_{BE} / \partial T \approx 1.5 \text{ mV/K}$.

B. Positive-TC Voltage

If two bipolar transistors operate at unequal current densities, then the difference between their base-emitter voltages is directly proportional to the absolute temperature [1]. As shown in Fig. 2, if two identical transistors ($I_{S1} = I_{S2}$) are biased at collector currents of nI_0 and I_0 and their base currents are negligible. From the equation $I_C = I_S \exp(V_{BE} / V_T)$, then $V_{BE} = V_T \ln \frac{I_C}{I_S}$. Therefore, the equation (10), (11) and (12) are obtained.

$$\Delta V_{BE} = V_{BE1} - V_{BE2} \quad (10)$$

$$= V_T \ln \frac{nI_0}{I_{S1}} - V_T \ln \frac{I_0}{I_{S2}} \quad (11)$$

$$= V_T \ln n \quad (12)$$

Thus, the V_{BE} difference exhibits a positive temperature coefficient as follow (13).

$$\frac{\partial \Delta V_{BE}}{\partial T} = \frac{\kappa}{q} \ln n \quad (13)$$

This TC is independent of the temperature or behavior of the collector current. Specially, when the circuit likes that shown as in Fig. 3, neglecting I_B (base current), the equation can be written as (14) and (15).

$$\Delta V_{BE} = V_T \ln \frac{nI_0}{I_{S1}} - V_T \ln \frac{I_0}{mI_{S2}} \quad (14)$$

$$= V_T \ln nm \quad (15)$$

C. Bandgap Reference

With the negative- and positive-TC voltages obtained above, a reference having a nominally zero temperature coefficient can be developed. The equation is written as follow

$$V_{REF} = \alpha_1 V_{BE} + \alpha_2 (V_T \ln n)$$

where $V_T \ln n$ is the difference between the base-emitter voltages of the two bipolar transistors operating at different current densities. Since at room temperature $\partial V_{BE} / \partial T \approx -1.5 \text{ mV/}^\circ \text{K}$ whereas $\partial V_T / \partial T \approx +0.087 \text{ mV/}^\circ \text{K}$, we may set $\alpha_1 = 1$ and choose $\alpha_2 \ln n$ such that $(\alpha_2 \ln n)(0.087 \text{ mV/}^\circ \text{K}) = 1.5 \text{ mV/}^\circ \text{K}$. That is, $\alpha_2 \ln n \approx 17.2$, indicating that for zero TC:

$$V_{REF} \approx V_{BE} + 17.2 V_T \approx 1.25 V \quad (16)$$

As shown in Fig. 2, it is an implementation accomplishing both to guarantee $V_X = V_Y$ and to arrive at a current equal to $V_T \ln n / R_3$ through the right branch, because of $V_{BE1} - V_{BE2} = V_T \ln n$, and hence an output voltage of the reference voltage is obtained as follow (17):

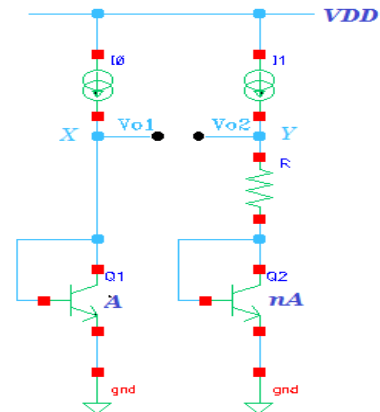


Fig. 2. Conceptual generation of temperature-independent voltage.

$$V_{out} = V_{BE2} + \frac{V_T \ln n}{R_3} (R_2 + R_3) \quad (17)$$

$$= V_{BE2} + V_T \ln n \left(1 + \frac{R_2}{R_3}\right) \quad (18)$$

For a zero TC, $\left| V_T \ln n \left(1 + \frac{R_2}{R_3}\right) \right| \gg 17.5$ must be obtained by $n=31$ and $R_3 / R_2 = 4$.

D. Collector Current Variation

From Fig. 2, if the collector current of Q1 and Q2, given by $(V_T \ln n) / R_3$, are PTAT, whereas $\partial V_{BE} / \partial T = -1.5mV / ^\circ K$ was derived for a constant current, then the formation (19) can be obtained by $I_{C1} = I_{C2} \approx (V_T \ln n / R_3)$.

$$\frac{\partial V_{BE}}{\partial T} = \frac{\partial V_T}{\partial T} \ln \frac{I_C}{I_S} + V_T \left(\frac{1}{I_C} \frac{\partial I_C}{\partial T} - \frac{1}{I_S} \frac{\partial I_S}{\partial T} \right) \quad (19)$$

Since $\partial I_C / \partial T \approx (V_T \ln n) / R_3 T = I_C / T$, so (19) can be written as (20)

$$\frac{\partial V_{BE}}{\partial T} = \frac{\partial V_T}{\partial T} \ln \frac{I_C}{I_S} + \frac{V_T}{T} - \frac{V_T}{T} \frac{\partial I_S}{\partial T} \quad (20)$$

Therefore equation (9) is modified as (21), indicating that TC is slightly negative than $-1.5mV / ^\circ K$.

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_{BE} - (3 + m)V_T - E_S / q}{T} \quad (21)$$

E. Compatibility with CMOS Technology

In n -well processes, a pnp transistor can be formed as depicted in Fig. 3 in which exhibits the exponential characteristics of bipolar devices for both negative and positive-TC quantities on which the derivation of a temperature-independent voltage relies.

A $p+$ diffusion inside an n -well serves as the emitter and the n -well itself as the base. The p -substrate acts as the collector and it is inevitably connected to the most negative supply that is usually ground. So the nnp in Fig. 2 can be replaced by pnp of which base and emitter are grounded.

F. OPAMP Offset and Output Impedance

The output voltage of the OPAMP is not zero if the input is set to zero because of asymmetries, OPAMPs suffer from input "offsets". As shown in Fig. 4, the input offset voltage of the OPAMP introduces errors in the output voltage, which is quantified as $V_{BE1} - V_{OS} \approx V_{BE2} + R_3 I_{C2}$ (if A_I is large) and $V_{out} = V_{BE2} + (R_3 + R_2) I_{C2}$. Thus,

$$V_{out} = V_{BE2} + (R_3 + R_2) \frac{V_{BE1} - V_{BE2} - V_{OS}}{R_2} \quad (22)$$

$$= V_{BE2} + \left(1 + \frac{R_2}{R_3}\right) (V_T \ln n - V_{OS}) \quad (23)$$

where assuming $I_{C2} \approx I_{C1}$ despite the offset voltage. The result is that V_{OS} is amplified by $1 + \frac{R_2}{R_3}$, introducing errors in V_{out} . More importantly, V_{OS} itself varies with

temperature, raising the temperature coefficient of the output voltage [2].

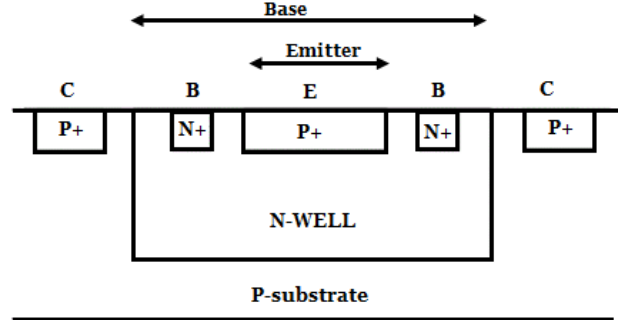


Fig. 3. Realization of a pnp bipolar transistor in CMOS technology.

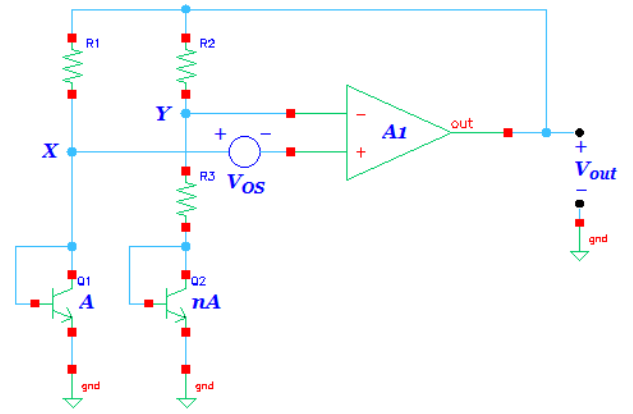


Fig. 4. Effect of OPAMP offset on the reference voltage.

G. Other Elements

Feedback Polarity: The feedback signal produced by the OPAMP in the circuit of Fig. 2 returns to both of its input. The negative feedback factor is given by (24).

$$\beta_N = \frac{1/g_{m2} + R_3}{1/g_{m2} + R_3 + R_2} \quad (24)$$

And the positive feedback factor by (25).

$$\beta_P = \frac{1/g_{m1}}{1/g_{m1} + R_1} \quad (25)$$

To ensure an overall negative feedback, β_P must be less than β_N , perfectly by roughly a factor of two so that the circuit's transient response remains well-behaved with large capacitive loads.

Bandgap Reference: The voltage generated according to (16) is called a "bandgap reference". The output voltage is written as follow:

$$V_{REF} = V_{BE} + V_T \ln n \quad (26)$$

And hence:

$$\frac{\partial V_{REF}}{\partial T} = \frac{\partial V_{BE}}{\partial T} + \frac{\partial V_T}{\partial T} \ln n \quad (27)$$

Setting this to zero and substituting for $\frac{\partial V_{BE}}{\partial T}$ from (9), (28) can be obtained.

$$\frac{V_{BE} - (4 + m)V_T - \frac{E_g}{q}}{T} = -\frac{V_T}{T} \ln n \quad (28)$$

(29) can be obtained from (26) and (28).

$$V_{REF} = \frac{E_g}{q} + (4 + m)V_T \quad (29)$$

Supply Dependence and Start-Up: As shown in Fig. 2, the output voltage is relatively independent of the supply voltage so long as the open-loop gain of the OPAMP is sufficiently high. The circuit may require a start-up mechanism because if V_X and V_Y are equal to zero, the input differential pair of the OPAMP may turn off.

IV. MISMATCH

In general, the mismatches caused by manufacturing processes can be classified into systematic mismatch and random mismatch. The random mismatch can only be reduced by increasing layout area, but the systematic mismatch can always be alleviated through proper layout techniques [3].

Expressing the characteristics of a MOSFET in saturation as $I_D = (1/2)\mu C_{ox}(W/L)(V_{GS} - V_{TH})^2$, mismatches between μ , C_{ox} , W , L , and V_{TH} result in mismatch between drain current (for a given V_{GS}) or gate-source voltages (for a given drain current) of two nominally-identical transistors. It is assumed that the dominating effects in random mismatches of a transistor are two independent variables: current factor differences $\Delta\beta$ ($\beta = \mu C_{ox}W/L$) and threshold voltage differences ΔV_{TH} . (30) and (31) are obtained.

$$\Delta\beta = \frac{A_K}{\sqrt{WL}} \quad (30)$$

$$\Delta V_{TH} = \frac{A_{V_{TH}}}{\sqrt{WL}} \quad (31)$$

where $A_{V_{TH}}$ and A_K are proportionality factors. $A_{V_{TH}}$ has been observed to scale down with the gate oxide thickness [4]. Mismatch lead to three significant phenomena: dc offset, finite even-order distortion, and lower common-mode rejection.

V. LAYOUT MATCHING

As previously analyzed and modeled, V_{REF} , I_D are always mismatched by μ , C_{ox} , W , L , and V_{TH} . Simple layout are prone to process variation, e.g. V_{TH} , KP , C_{ox} . Matched transistor requires elaborated layout techniques.

A. Layout Matching for Two Current Sources

The widely used approach for predicting the effects of the threshold voltage gradient is based upon deriving an equivalent threshold voltage for the device as given by the following equation [5].

$$V_{Theq} = \frac{\iint_{Active_Area} V_{TH}(X, Y) dx dy}{Active_Area} \quad (32)$$

where V_{Theq} can be viewed as the equivalent threshold voltage at the moment of the device. The most interesting topology is shown in Fig. 5. With totally four symmetric axes, its performance is definitely better than those of other topology [6], [9]. And the Four-Segment layout has the performance as shown in TABLE I. Assuming that the mismatch of the threshold voltage is equally distributed between the M1 and M2 transistors, the first-order expression of the current ratio is obtained as follows (33)

$$\frac{I_O}{I_{D1}} = 1 - \frac{2\Delta V_{THN}}{(V_{GS} - V_{THN})} \quad (33)$$

From (32), with the decrease of V_{GS} , the offset between current will increase due to the mismatch of threshold voltage. Because the threshold voltage is very sensitive to the gradient variation of process parameters, the current deviation caused by the threshold voltage mismatch will be especially serious when the distance between MOS transistors is very large [8].

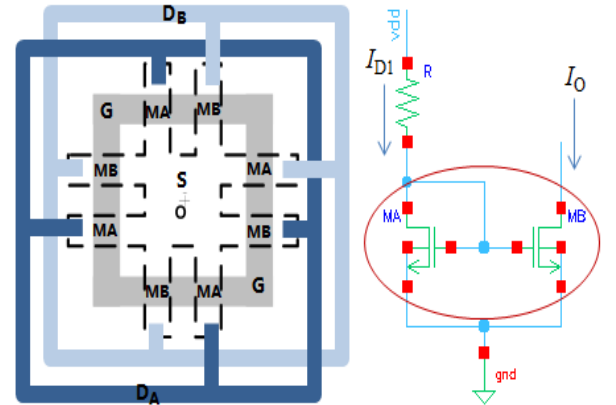


Fig. 4. Four segment rectangular layout.

TABLE I: THE PERFORMANCE OF FOUR-SEGMENT LAYOUT

Simple integral model	Worst Mismatch (%)		Effective Resolution
	Segmented integral model	Distributed simulator	
0	2.0966e-14	1.4090e-4	18-bit

B. Layout Matching for Differential Pair

The performance of the differential pair is closely related to the matching between the devices. Using the centroid layout technology, the first order mismatch caused by oxide gradient, stress gradient and other process deviations is minimization.

An algorithm that is used to determine the number of rows and columns required for the matrix is based on the following equation (34) [7].

$$A_r = \frac{2 \cdot W_{total} + R \cdot C \cdot K_3}{C^2 \cdot K_1 + C \cdot K_2} \quad (34)$$

where A_r is the aspect ratio, W_{total} is the total width of the largest transistor, R is number of rows, C is the number of columns, K_1 is a function of the transistor length, K_2 corresponds to the space for vertical routing, and K_3 is the space for horizontal routing. C (column) can then be determined using a optimization algorithm based on the requirements that the number of columns is even and both the number of R and C are integers [8]. Fig. 5 illustrates the layout of the differential input pair. Note that each device has the exact same metal and poly routing and that the layout is completely symmetrical about the center of the circuit.

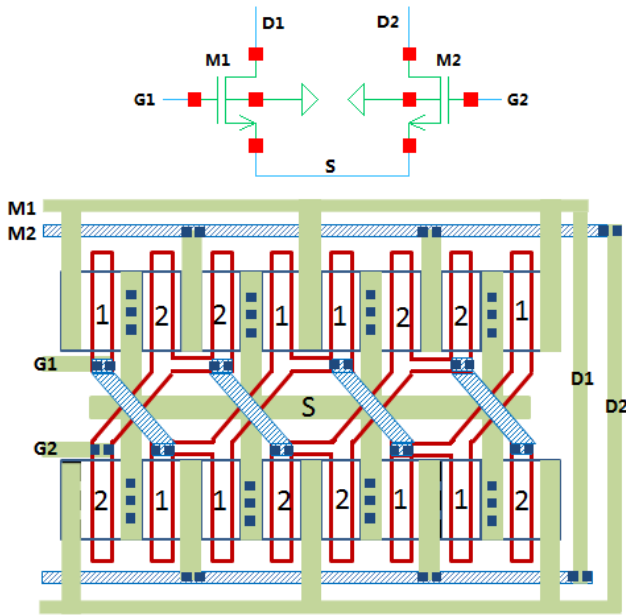


Fig. 5. Interdigitated differential input pair layout.

The offset voltage V_{OS} of the differential input pair caused by the mismatch of threshold voltage ΔV_{THN} , geometric size $\Delta(W/L)$ and load resistance ΔR_L can be calculated by (35).

$$V_{OS} = \Delta V_{THN} + \frac{V_{GS} - V_{THN}}{2} \left[\frac{-\Delta R_L}{R_L} - \frac{\Delta(W/L)}{(W/L)} \right] \quad (35)$$

The mismatch of threshold voltage must be reduced by optimized layout design. The mismatch between geometric size and load resistance can be reduced by using smaller V_{GS} (making V_{GS} close to V_{THN}). This conclusion can be compared with (32). (32) is shown that the use of smaller V_{GS} in current mirrors will lead to larger current mirror errors.

C. Other Layout Matching

Another layout matching technique is that the dummy MOS on the ends of the rows used to reduce the undercutting of the gate oxide on the end devices.

Latchup is a parasitic effect in CMOS technology, it is a PNP parasitic structure formed by at least two coupled bipolar transistor. When a transitory voltage/current overshoot/undershoot at a input/output node occurs, PNP structure can be turned on and a low impedance guarding

structures are used in order to prevent the latchup effect.

VI. A CASE STUDY OF BANDGAP REFERENCE

As shown in Fig. 6, it is a bandgap reference circuit used for LDO(Low-Drop linear regulator). And Its corresponding layout is shown in Fig. 7.

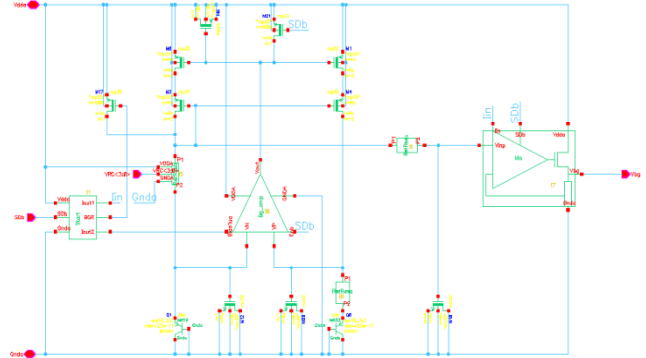


Fig. 6. A Bandgap reference circuit.

After analysis and design, the layout results are ideal. Post simulation were showed that the output reference voltage was 1.2156 and its temperature coefficient was $0.43 \times 10^{-6}/^\circ\text{C}$ at the range of $-40^\circ\text{C} \sim 125^\circ\text{C}$. The power supply rejection ratio (PSRR) was lower than -83dB at low frequency.

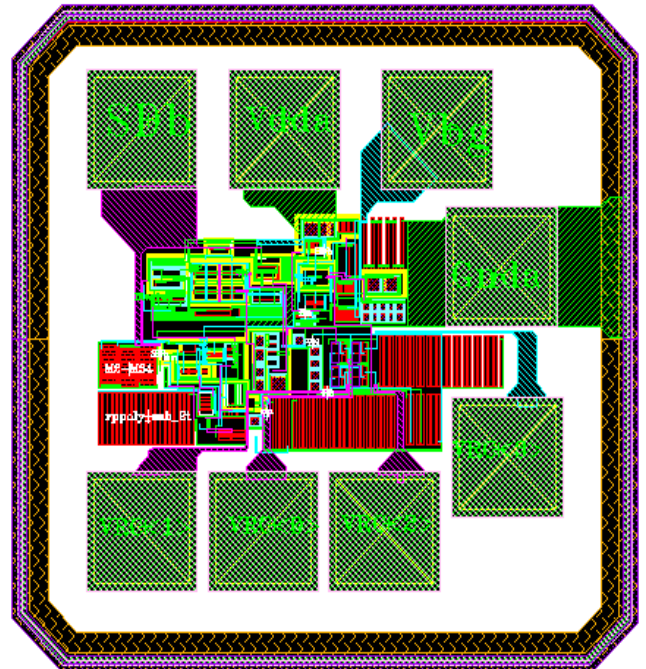


Fig. 7. Bandgap reference layout.

VII. CONCLUSION

A practical case study of bandgap reference is studied from analysis, design to layout implementation. The study shows that V_{BE} , threshold voltage and V_{GS} are important factors affecting bandgap reference, and shows how to analyze and design layout to satisfy these circuit requirements. The simulation results & layout can provide design reference for circuit or layout engineer.

REFERENCES

- [1] D. Hibber, "A new semiconductor voltage standard," *ISSCC Dig. of Tech, Papers*, pp. 32-33, Feb.1964.
- [2] B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill, 2001 pp. 463-479.
- [3] A. Hastings, *The Art of Analog Layout*, 2nd Ed. Pearson Education, Inc, publishing as Prentice Hall, 2006, pp. 220-259.
- [4] M. J. M. Pelgrom, A. C. J. Duijnmaier, and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE J.Solid-State Circuits*, vol. SC-24, pp. 1433-1439, Oct 1989.
- [5] M. F. Lan, A. Tammineedi, and R. Geiger, "A new current layout technique for improved matching characteristics," in *Proc. MWSCAS*, Aug. 1999, pp. 1126-1129.
- [6] Y. H. Jen, M. H. Chiang, C. C. Chen, and P. Chen, "A perfect matching layout for multiple cascode current sources," in *Proc. 2005 WSEAS Int. Conf. on Dynamical Systems and Control*, Venice, Italy, Nov. 2-4, 2005, pp. 529-534.
- [7] J. D. Bruce, H. W. Li, M. J. Dallabetta, and R. J. Baker, "Aanlog layout using ALAS," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 2, Feb. 1996.
- [8] R. J. Baker, H. W. Li, and D. E. Boyce, *CMOS Circuit Design, Layout, and Simulation*, John Wiley & Sons, Inc., 2003, pp. 340-344/454-464.
- [9] P. G. Drennan and C. C. McAndrew, "Understanding mosfet mismatch for analog design," *IEEE Journal of Solid-Tate Circuit*, vol. 38, no. 3, March 2003.



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