

Design of a High Frequency Duty-Cycle Corrector within 20%–80% Correction Range

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Abstract—An analog duty cycle correction circuit using a novel pulse-width modification cell. We correct the duty-cycle by changing the phase of the voltage. Our calibration allows the input duty cycle to range from 20% to 80%, and the circuit corrects the duty cycle to 50%. The proposed circuit operation frequency is at 0.8GHz to 4GHz, and it corrects to less than 1% error.

The duty-cycle correction circuit is implemented in a 1.8V, and 180nm CMOS technology at 25 °C.

Index Terms—Duty-cycle corrector, high frequency, wide range.

I. INTRODUCTION

As the high-speed circuits and systems increases, the duty cycle must be precisely at 50%. But the duty cycle will not be exactly 50% due to the effects of process, voltage and temperature (PVT) [1]-[4]. As a result, how to overcome the error of duty cycle is an important issue. The traditional analog DCC circuit uses an analog integrator to detect the duty cycle error, but this can only be used in low speed applications [5]. The digital DCC uses two delay lines to correct the accuracy [6], [7]. This requires a very complicated circuit and results in relatively high power consumption [8]. So, we propose a circuit to correct the duty cycle.

It can make the correction frequency higher and have a larger correction range. Because this structure is highly symmetrical, it can reduce the impact of PVT to very low.

This circuit consists of three parts. The first part is a duty cycle adjuster (DCA), the second part is a buffer, and the third part is a duty cycle detector (DCD).

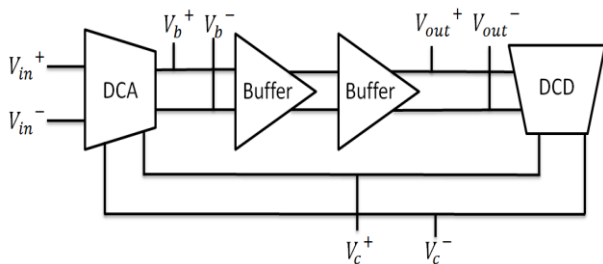


Fig. 1. Duty cycle correction circuit block.

II. CIRCUIT DESIGN

Fig. 1 shows the architecture of the proposed analogue DCC. The circuit we propose is a differential pair. The differential input enters DCA because resistance R1 and R2 make the amplitude smaller. So we add a Buffer to make the amplitude change back to what we need. The DCD is a

combination of a low-pass filter and an Integrator. The signal passes through the LPF to cause a DC voltage, and the DC voltage is feedback to the DCA through the Integrator to correct the circuit.

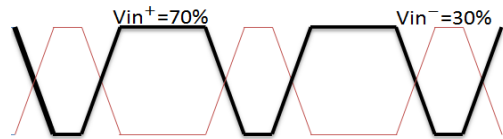


Fig. 2. (a) $V_{in+}=70\%$ $V_{in-}=30\%$.

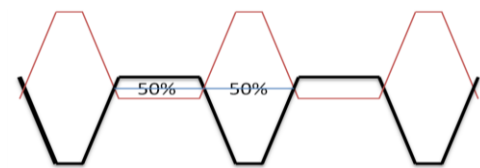


Fig. 2. (b) V_c feedback makes shift.

A. Duty Cycle Adjuster

Fig. 3 shows the circuit diagram of DCA. Transistors M5 and M6 as current sources.

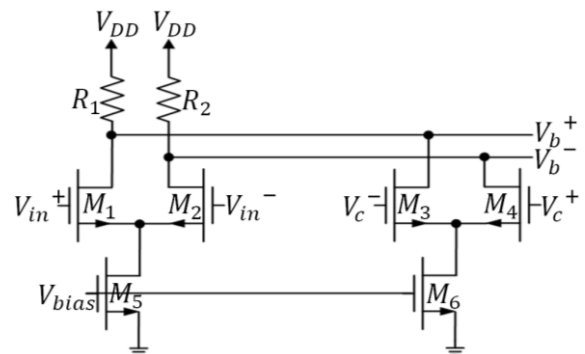


Fig. 3. Duty cycle adjuster circuit diagram.

Current $I_{R1} + I_{R2} = I_{M5}$. If R_1 and R_2 are the same size, I_1 and I_2 will be the same.

The resistance R will cause the original input signal peak to change from 0V to 1.8V to $0.7V \sim (1.8 - I_2 R_2)V$

Fig. 4 shows the change of the input voltage through DCA.

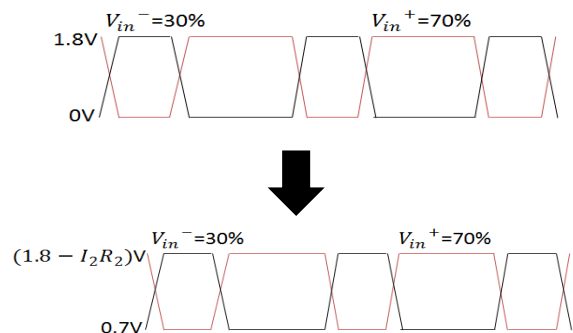


Fig. 4. Voltage change.

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B. Buffer

Fig. 5 shows the circuit composition of the Buffer. Proposed Buffer is composed of two inverters.

The buffer is to buffer the voltage that was just reduced in the Duty cycle adjuster.

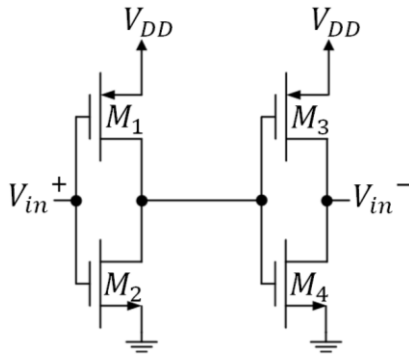


Fig. 5. Buffer circuit diagram.

Fig. 6 shows the change of the input voltage through Buffer

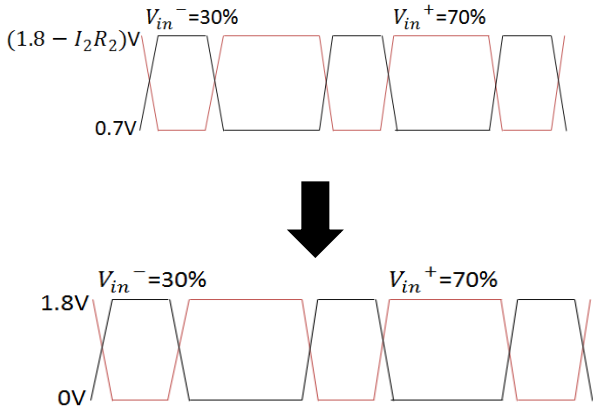


Fig. 6. Voltage change.

C. Duty Cycle Detector

Fig. 7 shows the circuit diagram of DCD. Function is to create a stable DC voltage.

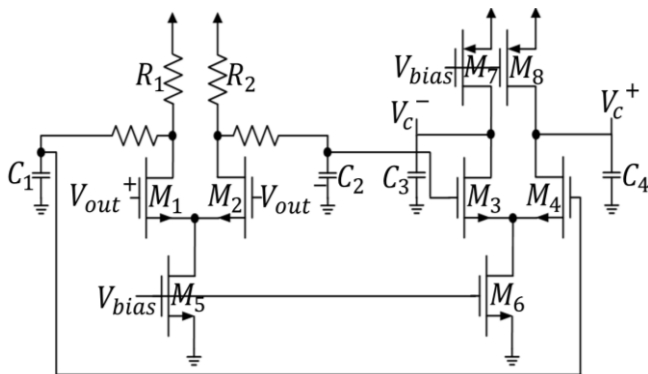


Fig. 7. DCD.

It consists of an integrator and a low pass filter. The function of the integrator is to integrate the input waveform into a stable DC voltage.

If the input duty cycle is 50%, the output is the same voltage. If the input duty cycle is not 50%, the output is not the same voltage. The voltage will reflux to duty cycle adjuster.

For example :

(1)
 $input^+ = 50\%$ than $output^+ = 1.8V * 50\% = 0.9V$
 $input^- = 50\%$ than $output^- = 1.8V * 50\% = 0.9V$
 They have same output voltage

(2)
 $input^+ = 70\%$ than $output^+ = 1.8V * 70\% = 12.6V$
 $input^- = 30\%$ than $output^- = 1.8V * 30\% = 0.54V$
 They have different output voltage

III. ALL CIRCUIT DIAGRAM

Fig. 8 shows the whole circuit diagram, using differential input signal, the signal is reduced by DCA, and then the waveform is restored by BUFFER, and then the DC voltage is returned to DCA for correction by DCD.

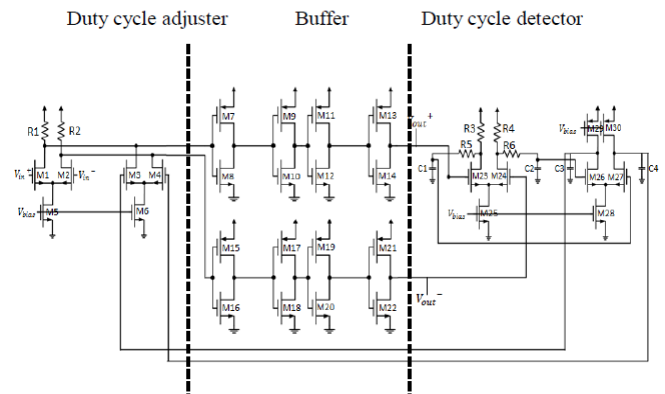


Fig. 8. All architecture.

IV. CALIBRATION PROCESS

(i) Fig. 9 shows the waveform shrinks when the input signal passes through the DCA. Signal peak to peak 0V ~ 1.8V to 0.7V ~ (1.8-I2R2)V

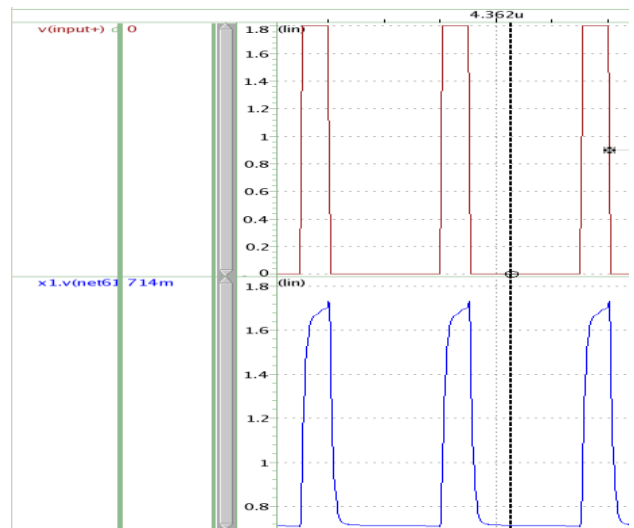


Fig. 9. The input signal passes through the DCA.

(ii) Fig. 10 shows that the reduced signal gradually returns after the Buffer. Single through buffer peak to peak 0.7V ~ (1.8-I2R2)V to 0V ~ 1.8V

(iii) Fig. 11 shows that at the beginning of the voltage, because the duty cycle is different, Vc+ and Vc- are different. After slowly correcting, Vc+ and Vc- will gradually become the same, and finally become the same voltage.

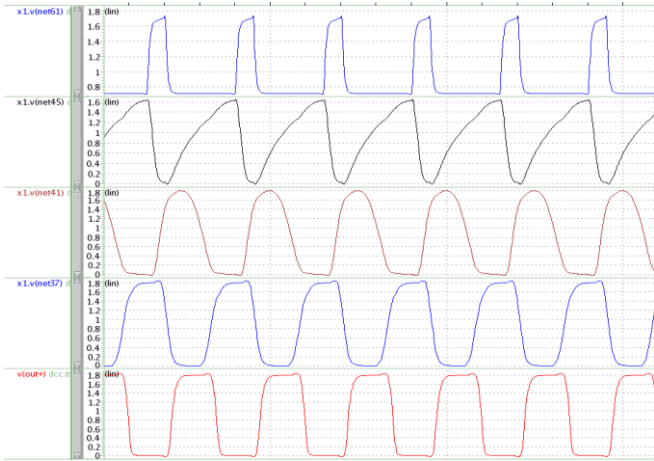


Fig. 10. The signal passes through the buffer.

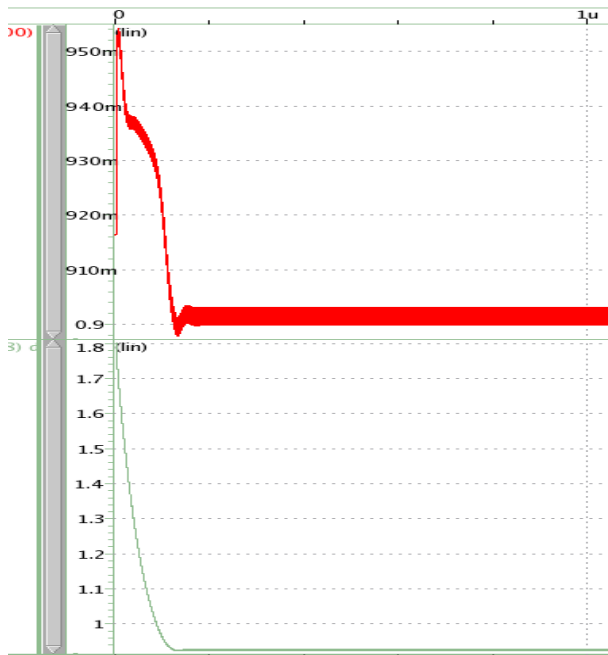


Fig. 11. The signal passes through the DCD.

V. RESULT

The proposed analog DCC circuit has been implemented in 180 nm CMOS technology with a 1.8 V supply. Fig. 6 shows the post-simulation input clock 30% and 70% at 0.8GHz and input clock 30% and 70% at 3GHz.

Fig. 12 to Fig. 15 show the simulation results of the circuit.

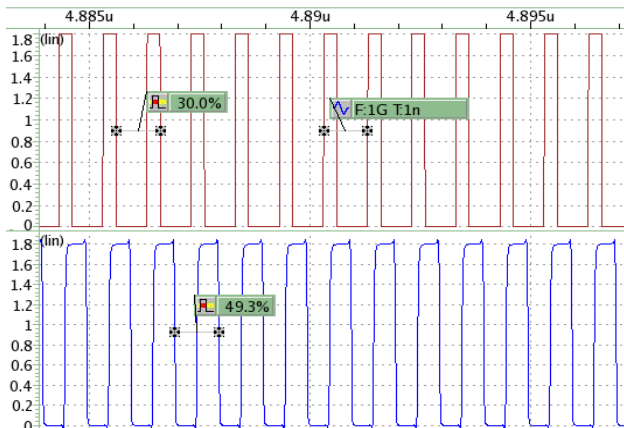


Fig. 12. Input 30% at 1 GHz.

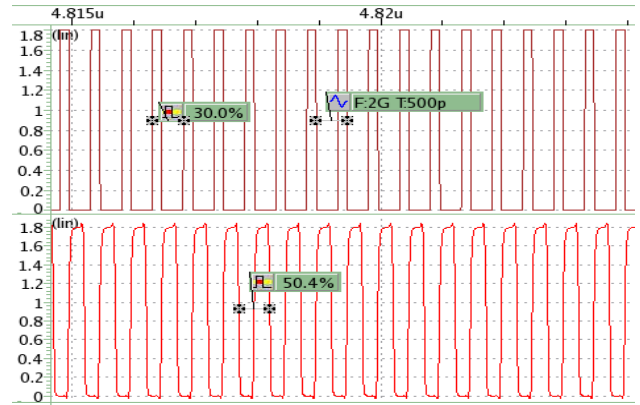


Fig. 13. Input 30% at 2 GHz.

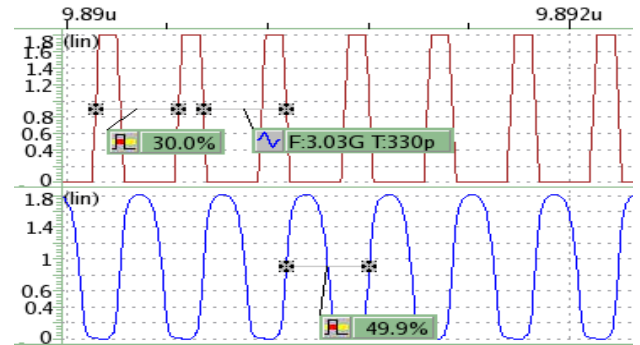


Fig. 14. Input 30% at 3.03 GHz.

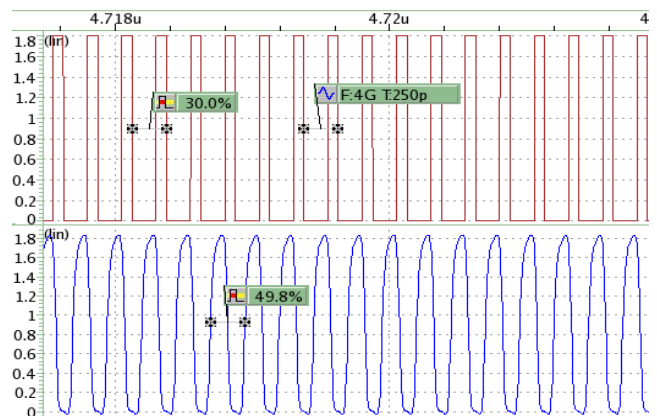


Fig. 15. Input 30% at 4 GHz.

Fig. 16 shows that after the simulation, it can be found that the correction range from 0.8GHz to 3GHz is relatively wide, and can be from 20% to 80%. But 3GHz to 4GHz can be corrected 30% to 70%

Fig. 17 shows a comparison of the proposed circuit diagram with other papers.

Fig. 18 shows the layout of circuit.

	400M	800M	1G	1.4G	2G	2.5G	3G	3.5G	4G
10%	20.1	29.9	34.5	42.8	49.1	60.7	X	X	X
20%	30.1	40.3	45.3	49.3	50.1	50.3	50.0	67.8	X
30%	40.1	48.6	49.3	50.0	50.5	50.8	50.5	50.4	49.8
40%	48.7	49.7	50.0	50.4	50.7	50.9	50.6	50.6	50.7
50%	50.4	50.7	50.7	50.8	50.8	50.7	50.4	50.4	50.5
60%	50.0	50.1	50.1	50.1	50.1	50.1	49.7	49.8	50.0
70%	49.0	49.6	49.8	49.8	49.7	49.7	49.4	49.5	49.1
80%	48.9	48.6	48.6	49.4	49.5	49.5	49.2	X	X
90%	48.8	48.4	48.2	48.0	49.4	X	X	X	X

Fig. 16. All pre-layout simulation.

	[1]	[2]	[3]	This Work
Architecture	Analogue feedback	Mixed-mode digital	Fully digital	Analogue feedback
Technology(μm)	0.18	0.13	0.18	0.18
Operating Frequency	1MHz~1.3GHz	321.5M~1GHz	0.8~1.25 GHz	0.8GHz~3GHz
Supply Voltage (V)	1.8	1.8	1.8	1.8
Power consumption	4.8mW at 1.3GHz	3.2mW at 1GHz	16mW at 1GHz	N/A
Correction range	30-70	40-60	40-60	20-80
Duty accuracy (%)	N/A	50 \pm 1	50 \pm 3	50 \pm 1
Chip area (mm^2)	0.057	0.048	0.0896	0.52

Fig. 17. Comparison chart.

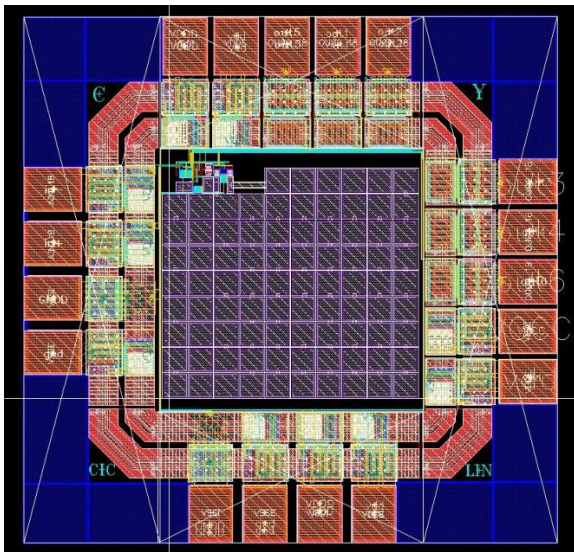


Fig. 18. Layout of DCC.

VI. CONCLUSION

We propose an analog DCC that can correct the bandwidth from 0.8GHz to 4GHz, the correction range can be 20% to 80%, and the correction to 50% accuracy is 1% or less. Plus its high Symmetrical structure can make it less affected by PVT. In the future, we hope to design a circuit that can also be corrected at higher frequencies.

In the post-layout simulation, because the parasitic capacitance and parasitic resistance are too much, the simulation result is not as expected. If the method of solving the parasitic parameters is found, the circuit will be more perfect.

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