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Two-Port SRAM Cell with Improved Write Operation

Wen-Chieh Wu, Ming-Chuen Shiau, Chien-Cheng Yu, and Ching-Chih Tsai

***Abstract*—It is well known that in Static Random Access Memory (SRAM) cells configured with single-ended bit lines, whenever a write operation is performed, a write failure may occur. In particular, it is relatively difficult to write a logical '1' to a cell if the cell currently stores a logical '0'. It is thus necessary to provide a method of resolving write failures in memory cells. In this paper, a novel seven-transistor (7T) two-port SRAM cell incorporating an assist circuit is proposed. Wherein, the assist circuit is used to deal with the memory cell failures. During a write operation, this circuit is activated to connect a diode-connected transistor to the source of the drive transistor located near to the write bit line. Accordingly, it can provide an efficient solution to the writing '1' issue to improve write operations in this manner. Simulation results for the proposed cell design confirm that there is a conspicuous improvement over the conventional two-port SRAM cells, and fast writing also can be achieved.**

***Index Terms*—Two-port, assist circuit, single-ended, static random access memory, read-write control circuit.**

I. INTRODUCTION

Generally, a memory device is classified into a DRAM (dynamic random access memory) and a SRAM according its respective data storage capability. DRAM is advantageous for its small size, but requires periodic refresh to prevent data loss. However, SRAM is advantageous for its simple operations, but occupies a large chip area. SRAM circuits are frequently used in most digital integrated circuits to store representations of data bits. SRAM circuits may be single-port or multi-port. In the single-port SRAM, normally, either of read and write operation is performed in one access from one port circuit connected to a pair of bit lines to one memory cell. The two-port SRAM, although it can perform a read and a write every clock cycle, requires more circuitry to perform the read and write operations. Fig. 1 shows a structure of a conventional six-transistor (6T) single-port SRAM [1]. The cross-coupled structure of inverters INV1 and INV2 ensures that logically opposite voltages are hold at storage nodes A and B, respectively.

One drawback of the conventional 6T SRAM cell is that its operation speed and cell size are strictly limited due to reliability concerns. Referring to Fig. 1, the drive transistor MN1 is made larger than the access transistor MA1 as such when both of these two transistors MN1 and MA1 are turned on, the drive transistor MN1 will have a lower resistance than the access transistor MA1. As a result, the drive transistor MN1 will more easily carry current when activated. However, for a successful write operation, it may be necessary that the access transistors should be very conductive to force the latch to change its equilibrium condition. Another drawback is that the data stored in the cells may be corrupted when the cells are read. For example, when a logical '0' is stored initially, the voltage rising in the cell may corrupt the data stored. Consequently, the access transistor should have a reduced conductivity for good stability in reading and standby operations. Therefore, the SRAM cell should provide less likely to be corrupted when the cell is read and more reliable when the cell is written [2]. These requirements impose contradicting requirements on transistor sizing. Recently, the cell ratio of the memory cell is reducing, this problem becomes more critical. One development is a two-port SRAM having dedicated read and write ports provides high speed read and write operations in place of the conventional single-port SRAMs [3]-[5].

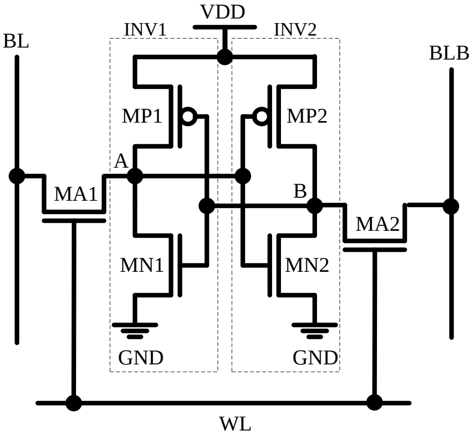

Fig. 1. Circuit diagram of the conventional 6T SRAM cell.

The remainder of this paper is organized as follows. Section II presents a brief description of a conventional 6T and an 8T two-port SRAM cell topologies. The proposed 7T two-port SRAM cell incorporating an assist circuit is described in Section III. The simulation results of the proposed 7T two-port SRAM cell are discussed in Section IV. Last section is a conclusion and summary for the paper.

II. EXISTING TECHNOLOGIES

The conventional 6T single-port SRAM cell can be modified to create a two-port SRAM cell. Two-port SRAM

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cell having dedicated read and write ports. Fig. 2 illustrates a conventional 6T two-port SRAM cell, which employs independent word lines (write word line WWL, read word line RWL) and bit lines (write bit line WBL, read bit line RBL) such that the opposite sides of the SRAM cell can be accessible by separate read and write ports [6]. The 6T two-port SRAM memory cell also includes an inverter INV1 mutually cross-coupled to an inverter INV2 to form a latch. The latch of the two-port SRAM itself has the same structure as that of the single-port SRAM, and therefore, the two-port SRAM has the same characteristics for read and write operations as the 6T single-port SRAM. In the write port, the write access transistor MA1 is dedicated exclusively to write operations. Moreover, in the read port, the read access transistor MA2 is devoted exclusively to read operations. In write operations, data is written into the SRAM cell by applying a logic high voltage signal to the write word line WWL, thereby turning the write access transistor MA1 on and coupling node A to the write bit line WBL. Alternately, data is read from the cell by applying a logic high voltage signal to the read word line RWL, thereby turning the read access transistor MA2 on and coupling node B to the read bit line RBL.

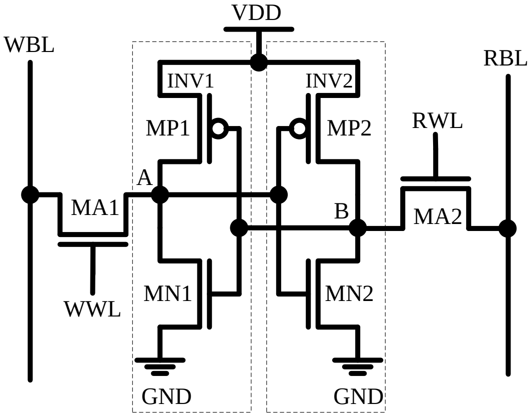

Fig. 2. Circuit diagram of the conventional 6T two-port SRAM cell.

Although the 6T two-port SRAM cell can be processed in the same manner as a conventional 6T single-port SRAM cell in write operations, a concern associated with the write operation is that it is relatively difficult to write a logical ‘1’ to the cell if the cell currently stores a logical ‘0’. The difficulty with write operations lies in the fact that it is very difficult to write a logical ‘1’ into the storage node A using only a single-ended write bit line structure [7], [8]. To provide full two-port memory functionality, several techniques have been developed [9]-[14]. These techniques usually increase or decrease a voltage applied to an individual memory cell. For example, boosting the voltage on a word line during a write cycle can improve the write margin of an SRAM memory cell. Lowering the voltage on a bit line below ground voltage during a write cycle can also improve the ability to write to a memory cell.

The conventional 6T single-port SRAM cell can also be made into an 8T two-port cell by inserting two additional transistors into the SRAM cell that implement a separate read port connected to a corresponding read bit line RBL and read word line RWL, as shown in Fig. 3 [9], [15]. The read port further comprises a read access transistor M14 and a read drive transistor M15 coupled in series to become a read stack. The reading of the data stored in SRAM cell is performed through the read access transistor M14 and the read drive transistor M15. The storage node A is coupled to the write bit line WBL through the write access transistor MA1, while the storage node B is coupled to the write bit line WBLB through the write access transistor MA2, wherein the storage nodes A and B are complementary nodes that are often at opposite voltage levels.

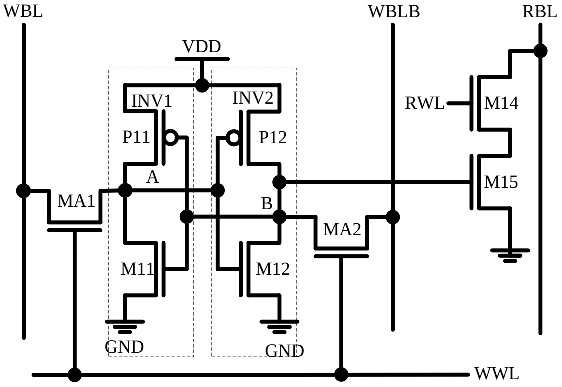

Fig. 3. Circuit diagram of the conventional 8T two-port SRAM cell.

Before a write operation is performed, the write word line WWL is asserted. In write operations, the read access transistor M14 is turned off, and the write access transistors MA1 and MA2 are turned on. Accordingly, the data value is written into cell through the write bit lines WBL and WBLB. Finally, at the end of the write operation, the write word line WWL is de-asserted, allowing the latch to function normally and hold the data of the storage node. It’s worth noting that, to guarantee a successful write operation, the storage node A must be pulled up (or down) above (or below) the trip-voltage of the inverter INV2 during the write word line WWL is asserted, otherwise a write failure will occur. Instead, when read operation is performed, the read bit line RBL is pre-charged during the read operation. Meanwhile, the write access transistors MA1 and MA2 are turned off, and the read access transistor M14 is turned on. If the storage node A is charged to a logic high, the read drive transistor M15 will be turned on and the voltage on the read bit line RBL will be pulled down to ground. On the contrary, if the storage node A is discharged to a logic low, the read drive transistor M15 will be turned off and the voltage on the read bit line RBL will be remained at its pre-charged level. Then, the sensing current on the read bit line RBL is detected by a sense amplifier (not shown) to determine the logic state of cell.

Advantageously, using the read-port of the 8T SRAM cell, the gate of the read drive transistor M15 receives the storage node voltage directly. Therefore, the data stored in the storage node B is not affected during the read operation through the read-port. Particularly, the read operation based on this read port has a characteristic in that this operation can be carried out completely independent of the write port, without destroying the data of the storage nodes A and B of the cell. However, the conventional 8T two-port SRAM cell has a large cell size due to eight transistors in total. As such, it is desirable to provide an SRAM cell that has the two-port functionality while maintaining a relatively small cell size.

III. PROPOSED TECHNOLOGY

Recently, several techniques have been developed to resolve the write ‘1’ issue of the SRAM cells configured with single-ended write bit line. Some of these techniques rely on boosted word line voltage [16]-[18], reducing the supply voltage VDD [19]-[21], sizing cell transistors [22], [23], and raising the source voltage V_{SS} [24], [25]. However, each of these techniques may cause a reduction in the drive current of the transistors and in the operating speed of the cell, or may increase memory cell area. Other techniques require generation of a voltage above the operating voltage, or require a more complicated circuit design and more complicated device process. Therefore, there is a need for an effective technique to improve the write operation of the SRAM cells configured with single-ended write bit line, which suffer from inability to write ‘1’.

A. The Proposed 7T Two-Port SRAM Cell Structure

The proposed 7T two-port SRAM cell structure includes a write port and a read port as shown in Fig. 4. The write port is configured to connect the latch, similar to that of the above-mentioned cells, to the write bit line WBL in response to a write signal on the write word line WWL for writing a logical state to the memory cell. The gate of the transistor M13 is connected to a corresponding write word line WWL for conveying a write signal. The memory cell further comprises a read port configured to read the logic state of the latch in response to a read signal on the read word line RWL. The read port of the cell includes a pair of series-connected NMOS transistors M14 and M15, wherein the gate of transistor M14 is connected to the read word line RWL and the gate of transistor M15 is coupled to the storage node B.

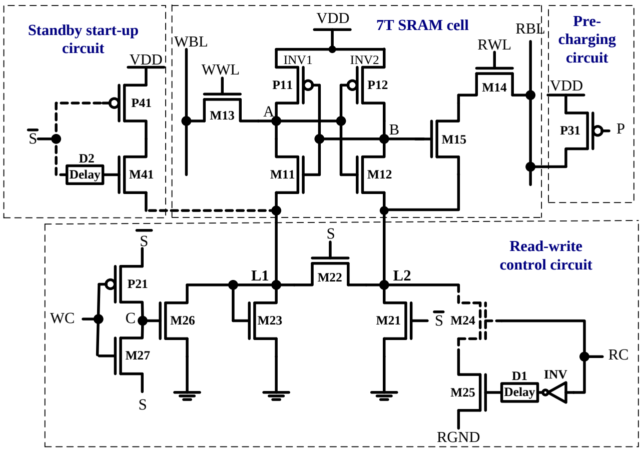

Fig. 4. Circuit diagram of the proposed 7T SRAM cell.

It’s worth noting that transistors P11 through P12 and M11 through M15 are appropriately sized to make the read and write states perform properly. Furthermore, the proposed cell structure also incorporates an assist circuit which consists of a read-write control circuit, a pre-charging circuit and a standby start-up circuit. Still referring to Fig. 4, the read-write control circuit is coupled to the source terminals corresponding to the drive transistors of each row memory cells. This configuration is aimed to control the source voltages of the drive transistors under different operating modes. That is, the read-write control circuit is configured to control the voltage levels of the nodes L1 and L2 (V_{L1} and V_{L2}, hereafter) in response to different operating modes. For example, during a read mode or during a standby mode, the read-write control circuit is configured to connect the voltage levels of the nodes L1 and L2 of the selected cell to ground. Further, during a write operation, the read-write control circuit is configured to provide the voltage of the node L1 with a NMOS threshold voltage, and the voltage of the node L2 with a ground voltage. In addition, the pre-charging circuit is connected to the read bit line RBL in each column. The function of the pre-charging circuit is to pull up the read bit line RBL of a selected column to V_{DD} before the read operation. Furthermore, the standby start-up circuit is to enable the SRAM cell to quickly switch to the standby mode, and thus effectively enhance the standby performance. In this manner, the memory cell has the advantages of having little or no adverse impact on cell stability or the write margin along with a relatively small cell size compared to the conventional two-port SRAM cells.

B. Write Operation

Referring again to Fig. 4, prior to the write operation is performed, the write control signal WC is at logic low, the transistor P21 is turned on and the transistor M27 is turned off. Thereby, the node C is at logic high and thus to turn on the transistor M26, as such the voltage V_{L1} is pulled down to the ground voltage. However, during the write operation, the signal WC is at logic high, the transistor P21 is turned off and the transistor M27 is turned on. Subsequently, the node C is at logic low and thus to turn off the transistor M26, as such the voltage V_{L1} is set to $V_{GS(M23)}$. Thus, the writing ‘1’ issue can be resolved. Fig. 5 shows the simplified circuit diagram during the write operation.

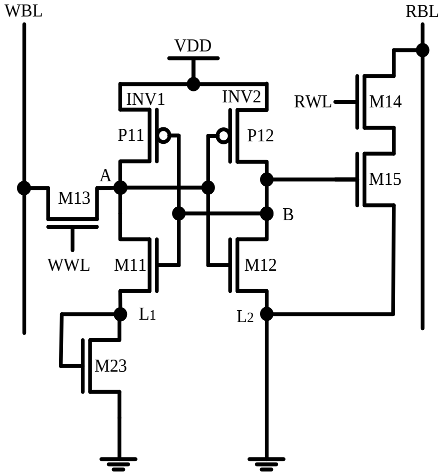

Fig. 5. The simplified circuit diagram during the write operation.

Referring to Fig. 5, before a write operation is performed, the write bit line WBL is pre-charged to a logic high. The logic state on the write bit line WBL can be inversed depending on the value to be written into the cell. And, the write word line WWL is then asserted to turn on the access transistor M13 allowing the data to be stored in the cell. When writing a logical ‘1’, the write access transistor M13 and the drive transistor M11 that together act as a voltage divider. As such, the node *A* will be charged toward the following voltage level:

$$V_{DD} \times \frac{R_{M11} + R_{M23}}{R_{M11} + R_{M13} + R_{M23}} \qquad (1)$$

where R_{M11}, R_{M13} and R_{M23} are the on-resistance of transistors M11, M13 and M23, respectively. At this moment, the transistor M13 is still in the saturation region and the transistor M11 in the triode region. Although R_{M13} may be greater than R_{M11}, the NMOS diode transistor M23 can provide a voltage $V_{GS\,(M23)}$ (i.e., the gate-source voltage of the transistor M23) at node L1. Consequently, to prevent the writing '1' issue during a write operation, the voltage V_{L1} of the selected cell is set to a predetermined voltage $V_{GS(M23)}$ which is higher than the ground voltage. Also, the voltage V_{L2} of the selected cell is set to the ground voltage.

IV. SIMULATION RESULTS

To evaluate performance, different SRAM cell structures discussed in this paper were simulated using a 0.18 um CMOS technology. All simulations were carried out at nominal conditions: V_{DD}=1.8V and at room temperature. The transients associated with a writing operation are detailed described below.

Firstly, consider the write '0' operation. Prior to the write '0' operation, the write word line WWL is at logic low. During the write '0' operation, if a logical '0' is stored previously, the write word line WWL transitions from a logic low to a logic high. As the voltage level of the write word line WWL (V_{WWL}) exceeds the threshold voltage of the transistor M13 (V_{TM13}), transistor M13 is turned on. Subsequently, owing to the fact that the voltage level of the write bit line WBL (V_{WBL}) is at logic low, the voltage V_A remains at the ground voltage. On the other hand, if a logical '1' is stored previously, when the write word line WWL transitions from a logic low to a logic high during the write '0' operation. As the voltage level of the write word line WWL (V_{WWL}) exceeds the threshold voltage V_{TM13}, transistor M13 is turned on. Subsequently, owing to the fact that the voltage level of the write bit line WBL (V_{WBL}) is at logic low, the node A and node L1 will be discharged to the ground until the end of the write '0' operation.

Secondly, consider the write '1' operation. Prior to the write '1' operation, the write word line WWL is at logic low. During the write '1' operation, if a logical '1' is stored previously, the write word line WWL transitions from a logic low to a logic high. As the voltage V_{WWL} exceeds the threshold voltage V_{TM13}, transistor M13 is turned on. Subsequently, owing to the fact that the voltage V_{WBL} is at logic high and transistor P11 still on, the voltage V_A remains at the power supply voltage V_{DD}. On the other hand, if a logical '0' is stored previously, the write word line WWL is at logic low and transistor M11 is turned on. It is to be noted that, since the transistor M11 is turned on, and therefore, when the write '1' operation is started, the write word line WWL transitions from a logic low to a logic high. The voltage at node A is slightly increased following the voltage of the write word line WWL due to the parasitic capacitance coupling effect. As the voltage V_{WWL} exceeds the threshold voltage V_{TM13}, transistor M13 is turned on. Subsequently, since the voltage V_{WBL} is at logic high and transistor M11 still on, and the voltage V_B remains at a voltage close to the power supply voltage V_{DD}, therefore, the transistor P11 remains off. As a result, the voltage at node A will rise up due to the voltage division along the drive and access transistors. When the voltage exceeds a threshold, it causes the bit to flip due to regenerative feedback. Hence, the write '1' operation is completed. It is worth noting that, when writing a logical '1' to a logical '0' is stored previously, the voltage V_{L1} is set to $V_{GS(M23)}$. After the completing of the write '1' operation, the voltage V_{L1} will be discharged to the ground voltage via transistor M26. Thus, the issue concerning the difficulty of writing '1' can be resolved. The simulated waveform of a successful writing in the proposed 7T SRAM cell is shown in Fig. 6.

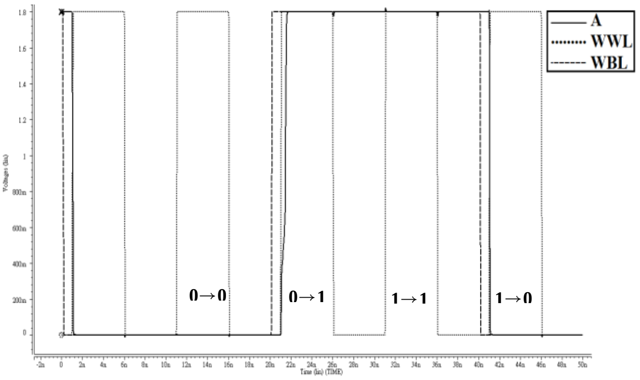

Fig. 6. Transient waveforms of a successful writing in the proposed 7T SRAM cell.

It is evident that the proposed 7T SRAM cell provides an efficient solution to the writing '1' issue, that is, the proposed 7T SRAM cell enabling a logical '1' to be easily written to the SRAM cell, as compared to the conventional two-port SRAM cells.

V. CONCLUSIONS

This paper has addressed the disadvantages of the existing two-port SRAM cells and further drawbacks inherent to single-ended bit line cells, and has provided an assist circuit for resolving the writing '1' issue. This assist circuit is activated to control the source voltages of the drive transistors in a different operating mode. In particular, in a write operation, the source terminal of the drive transistor located near to the write bit line is set to a positive threshold voltage. Meanwhile, the other drive transistor has its source terminal coupled to ground. Using this method, this design facilitates efficient writing of data into a single-ended write structure in an SRAM cell, particularly if a logical '0' stored in the cell is to be overwritten by a logical '1'. Simulation results for the proposed cell design confirm that the proposed cell provides an efficient solution to the writing '1' issue, that is, the proposed 7T SRAM cell enabling a logical '1' to be easily written to the SRAM cell. In addition, the proposed cell design also having the advantage of faster write operations without reducing cell stability.

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