A Proposal of a Hamming Distance Detector with a Neuron CMOS A/D Converter

Makoto Urakami, Masaaki Fukuhara, and Masahiro Yoshida

***Abstract*—In this paper, we propose a new Hamming distance detector using a neuron CMOS A/D converter with two output terminals. The detector outputs the signals which are corresponding to the Hamming distance between two input data immediately. The FPD method is applied to design the ratio of each input capacitance of the proposed detector. To verify the behavior of the proposed detector, the computer simulations were carried out by LTspice.**

***Index Terms*—A/D converter, hamming distance detector, neuron MOS.**

I. Introduction

The similarity of data is important in the fields of pattern matching and data comparison [1]. Hamming distance is one of the measures of the similarity. In the previous studies, the Hamming distance detectors of [2] and [3] determine whether the Hamming distance D_H between two input data is within a certain range or not by using threshold logic. These detectors have needed many reference signals and clock cycles.

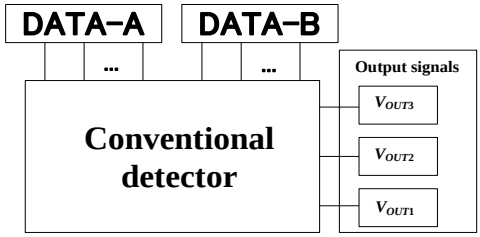

Fig. 1. Block diagram of conventional detector.

TABLE I: The Relationships of Hamming Distance and Output Signals of Conventional Detector

Hamming distance D_H	V_{OUT1}	V_{OUT2}	V_{OUT3}
0	0	0	0
1	0	0	1
2	0	1	1
More than 3	1	1	1

The other conventional detector determines the Hamming distance D_H between two input data with no reference signals immediately [4]. The block diagram of the conventional detector is shown in Fig. 1. The detector accepts DATA-A and DATA-B in parallel, and outputs 3-bit signals (V_{OUT1}, V_{OUT2} and V_{OUT3}) corresponding to the D_H between DATA-A and DATA-B as shown in Table I. The detector has required three output terminals, because it outputs 3-bit signals.

In this study, a new Hamming distance detector with a neuron CMOS A/D converter to reduce the number of output terminals is proposed. The block diagram of the proposed detector is shown in Fig. 2. The detector immediately determines the Hamming distance D_H between DATA-A and DATA-B with no reference signals and two output terminals. The relationships of D_H and 2-bit output signals (V_{OUT1} and V_{OUT2}) are shown in Table II. This detector separates the Hamming distance D_H into four states with employing only two output terminals instead of three output terminals.

The proposed detector is designed by using the FPD. FPD is a method to design the ratio of input capacitances in neuron CMOS circuit graphically. To verify the characteristics of the proposed detector, the computer simulations were carried out by LTspice.

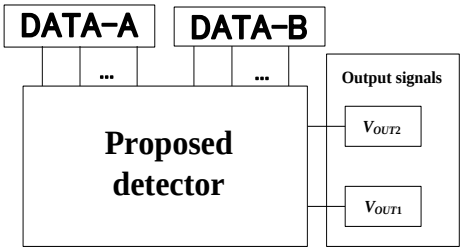

Fig. 2. Block diagram of proposed detector.

TABLE II: The Relationships of Hamming Distance and Output Signals of Proposed Detector

Hamming distance D_H	V_{OUT1}	V_{OUT2}
0	1	1
1	1	0
2	0	1
More than 3	0	0

II. Neuron CMOS Inverter

The proposed detector employs neuron CMOS inverters as an A/D converter. The construction of the neuron CMOS inverter is shown in Fig. 3. The neuron CMOS inverter consists of a nMOS, a pMOS, capacitors C_i (i=1, 2, …, n) and an ordinary CMOS inverter [5]. As shown in Fig. 3, the gate which is connected to the nMOS and pMOS is called floating gate. C_i (i=1, 2, …, n) represent the capacitances between the each input gate and the floating gate.

In the Fig. 3, V_i (i=1, 2, …, n) is the voltage applying the each input gate, Φ_F is the potential of the floating gate, V_{OUT} is the output voltage and V_{DD} is the power supply voltage.

Φ_F is determined by the capacitances C_i (i=1, 2, … , n) and the voltages V_i (i=1, 2, …, n) as shown by

$$\Phi_F = \frac{\sum_{i=1}^{n} C_i V_i}{\sum_{i=1}^{n} C_i} \quad (1)$$

Manuscript received July 9, 2014; revised September 11, 2014.

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DOI: 10.7763/IJIEE.2015.V5.507

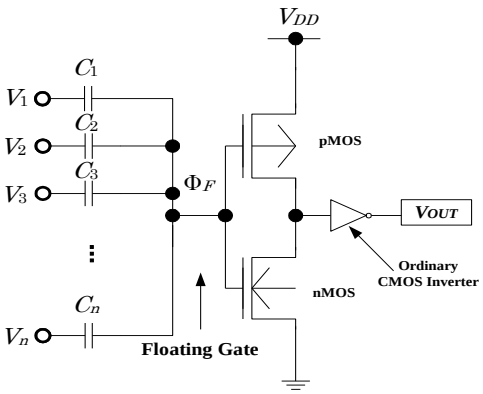


Fig. 3. Schematic diagram of neuron CMOS inverter.

The electrical charge of the floating gate is taken 0 and the capacitance between the substrate and the floating gate is ignored.

Operating states of the neuron CMOS inverter are determined by the relationships of the floating gate potential Φ_F and the inversion threshold voltage V_{INV} as seen from the floating gate. If Φ_F is less than V_{INV}, V_{OUT} becomes 0(V). If Φ_F is more than V_{INV}, V_{OUT} becomes V_{DD}.

III. Proposed Detector Configuration and Design Method

The schematic diagram of the proposed detector is shown in Fig. 4. The detector consists of an XOR array, a D/A converter and an A/D converter using two neuron CMOS inverters (Neuron CMOS1 and Neuron CMOS2). The XOR array is composed of n two-input XOR gates. The D/A converter has M_{N0}, M_{P0}, and M_{Nbi}(i=1, 2,…, n) , the Neuron CMOS1 has M_{N1}, M_{P1}, $C_{1,i}$(i=1, 2, 3) and an ordinary CMOS inverter, and the Neuron CMOS2 has M_{N2}, M_{P2}, $C_{2,i}$(i= 1, 2, 3, 4) and an ordinary CMOS inverter.

In the figure, A_i(i=1, 2,…, n) is a bit i of DATA-A, B_i(i=1, 2,…, n) is a bit i of DATA-B, M_{Ni} (i=0, 1, 2) and M_{Nbi}(i=1, 2,…, n) are the nMOS transistor, M_{Pi} (i=0, 1, 2) are the pMOS transistor, $C_{1,i}$ (i=1, 2, 3) and $C_{2,i}$ (i=1, 2, 3, 4) are the capacitance of each input gate of each neuron CMOS inverter, V_{ML} is the voltage of match line, V_{OUT1} and V_{OUT2} are the output voltages, $\overline{V_{OUT1}}$ is the input voltage of the ordinary CMOS inverter of the Neuron CMOS1 and V_{DD} is the power supply voltage.

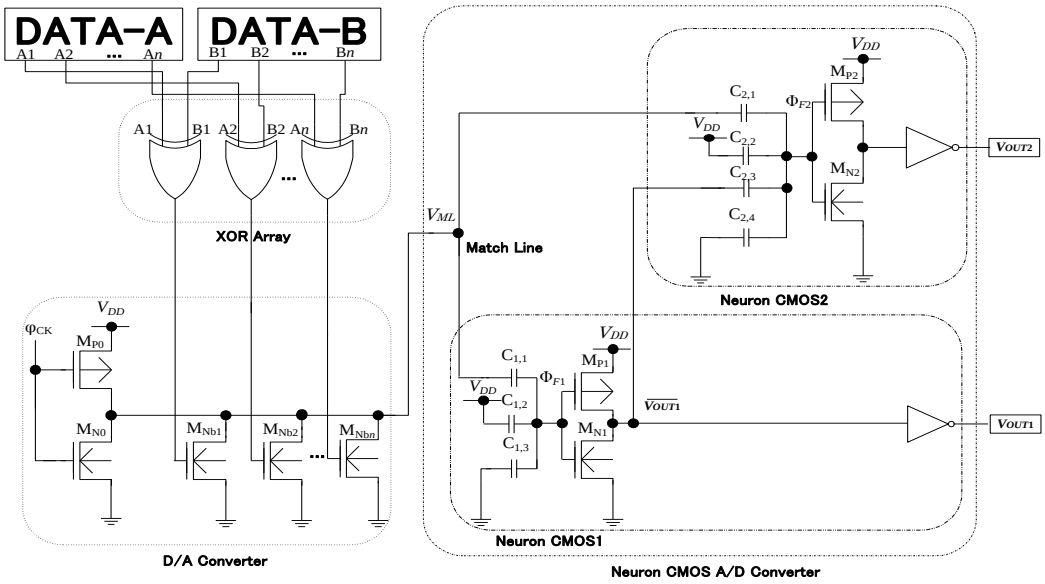


Fig. 4. Schematic diagram of a Hamming distance detector with a neuron CMOS A/D convert.

TABLE III: Device Parameters

	nMOS	pMOS	Unit
Threshold voltage	0.5	-0.8	V
Gate thickness	760	760	Å
Carrier mobility	421	159	cm^2/Vs

TABLE IV: Dimensions of MOS Transistors

Transistor name	W(μm)	L(μm)
M_{P0}	4.5	0.5
M_{N0},M_{Nb1},M_{Nb2},M_{Nb3}	1.0	0.5
M_{N1},M_{N2}	1.0	0.5
M_{P1},M_{P2}	4.35	0.5

When the clock signal φ_{CK} is low level, the detector operates the Hamming distance detecting operation. When φ_{CK} is high level, the detector operates the Reset operation.

At first, the two input data (DATA-A and DATA-B) of bit length n are applied to the XOR array. Each XOR determines whether the each bit is exact match or inexact match. If A_i(i=1, 2,…, n) equals B_i(i=1, 2,…, n), XOR outputs 0(V). If A_i(i=1, 2,…, n) and B_i(i=1, 2,…, n) are not equal, XOR outputs V_{DD}. In the detector, the number of inexact match bit is called Hamming distance D_H.

In the D/A converter, V_{ML} is determined corresponding to Hamming distance D_H. The relationships between D_H and V_{ML} which are obtained by the simulations are shown in Fig. 5. To analyze V_{ML}, computer simulations were carried out by LTspice with 0.35(μm) rules of TSMC. The device parameters are shown in Table III. The dimensions of the MOS transistors are shown in Table IV. Channel lengths L of all MOS transistors are constant at 0.5(μm). V_{DD} is 3.3(V).

In this paper, we design the ratio of the capacitance of the

each input gate of the neuron CMOS inverters when *n* equals 3 as an example by FPD (Floating gate Potential Diagram) [5]. If the Hamming distance D_H equals 0, then all M_{Nbi} (i=1, 2,…, n) are off. Therefore V_{ML} is V_{DD} when φ_{CK} is low level. V_{ML} decreases with increasing of the D_H if φ_{CK} is low level as shown in Fig.5. In the simulations, V_{ML} is 2.48(V) when D_H equals 1, 1.15(V) when D_H equals 2 and 0.68(V) when D_H equals 3.

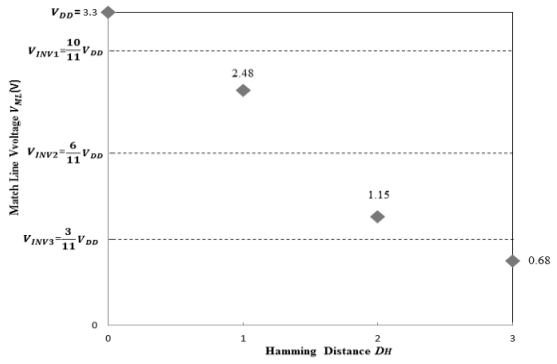


Fig. 5 Relationships between Hamming distance D_H and match line voltage V_{ML}

In this paper, noise margin is defined as a voltage width between the inversion threshold voltage V_{INV} of neuron CMOS inverter and V_{ML} of each distance. To make noise margin larger, V_{INV} is determined to the middle of V_{ML} in each distance. In the Fig. 5, each inversion threshold voltage V_{INVi}(i=1, 2, 3) are shown in the dotted line. From the figure, V_{INV1} is $\frac{10}{11}V_{DD}$, V_{INV2} is $\frac{6}{11}V_{DD}$ and V_{INV3} is $\frac{3}{11}V_{DD}$.

In the A/D converter, the output signals of Neuron CMOS1 $\overline{V_{OUT1}}$ and V_{OUT1} are determined corresponding to V_{ML}. The output signal of Neuron CMOS2 V_{OUT2} is determined corresponding to V_{ML} and $\overline{V_{OUT1}}$. The inversion threshold voltage of Neuron CMOS1 is V_{INV2}. The inversion threshold voltages of Neuron CMOS2 are V_{INV1}, V_{INV2} and V_{INV3}.

The FPD of Neuron CMOS1 represents the relationships of floating gate potential Φ_{F1}, V_{ML} and capacitances $C_{1,i}$(i=1, 2, 3) between the each input gate and the floating gate as shown in Fig. 6.

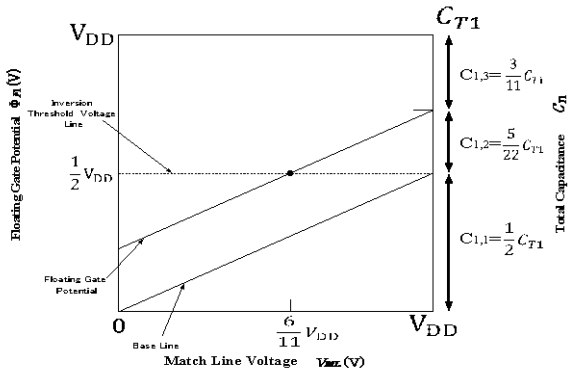


Fig. 6. FPD of Neuron CMOS1.

A vertical axis of left of Fig. 6 is the potential of floating gate Φ_{F1} of the Neuron CMOS1, a vertical axis of right is the total capacitance C_{T1} of each input gate of the Neuron CMOS1, and abscissa is V_{ML}. C_{T1} is the total capacitance of $C_{1,i}$(i=1, 2, 3). We assumed that the inversion threshold voltage as seen from the floating gate is $\frac{1}{2}V_{DD}$, and the inversion threshold voltage line is drawn in the FPD. Then the base line which is the potential of the floating gate when V_{ML} is varied from 0(V) to V_{DD} and the other control voltages are 0(V) is drawn. Based on the inversion threshold voltage V_{INV2} of the Neuron CMOS1, the potential Φ_{F1} of the floating gate corresponding to the V_{ML} is drawn. The ratio of each capacitance is indicated graphically as a split ratio of the vertical axis of right. Hence, the ratio of the capacitances of the Neuron CMOS1 is $C_{1,1} : C_{1,2} : C_{1,3} = 11 : 5 : 6$ as shown in Fig. 6.

The FPD of the Neuron CMOS2 is shown in Fig. 7. In the Fig. 7, a vertical axis of left is the potential Φ_{F2} of the floating gate of Neuron CMOS2, a vertical axis of right is the total capacitance C_{T2} of each input gate of the Neuron CMOS2 and abscissa is V_{ML}. C_{T2} is the total capacitance of $C_{2,i}$(i=1,2,3,4). Based on the inversion threshold voltages V_{INV1}, V_{INV2} and V_{INV3} of the Neuron CMOS2, the potential Φ_{F2} corresponding to the V_{ML} is drawn in Fig. 7. From the figure, the ratio of the capacitances of the Neuron CMOS2 is $C_{2,1} : C_{2,2} : C_{2,3} : C_{2,4} = 11 : 1 : 7 : 3$.

We designed the capacitances of the input gates as shown in Table V from the FPDs.

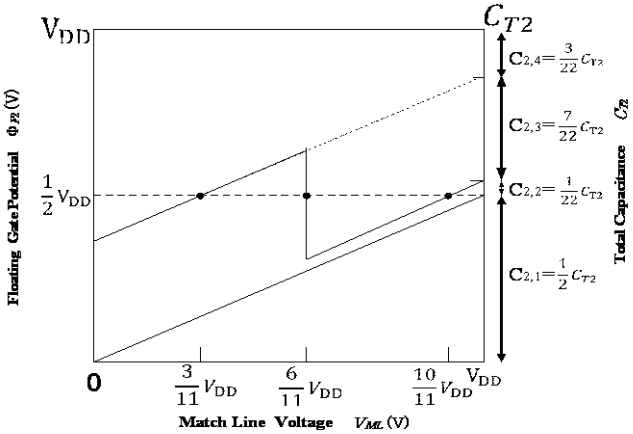


Fig. 7. FPD of neuron CMOS2.

TABLE V: CAPACITANCES OF EACH INPUT GATE OF NEURON CMOS1 AND NEURON CMOS2

Capacitor name	C(fF)
$C_{1,1}$	220
$C_{1,2}$	100
$C_{1,3}$	120
$C_{2,1}$	220
$C_{2,2}$	20
$C_{2,3}$	140
$C_{2,4}$	60

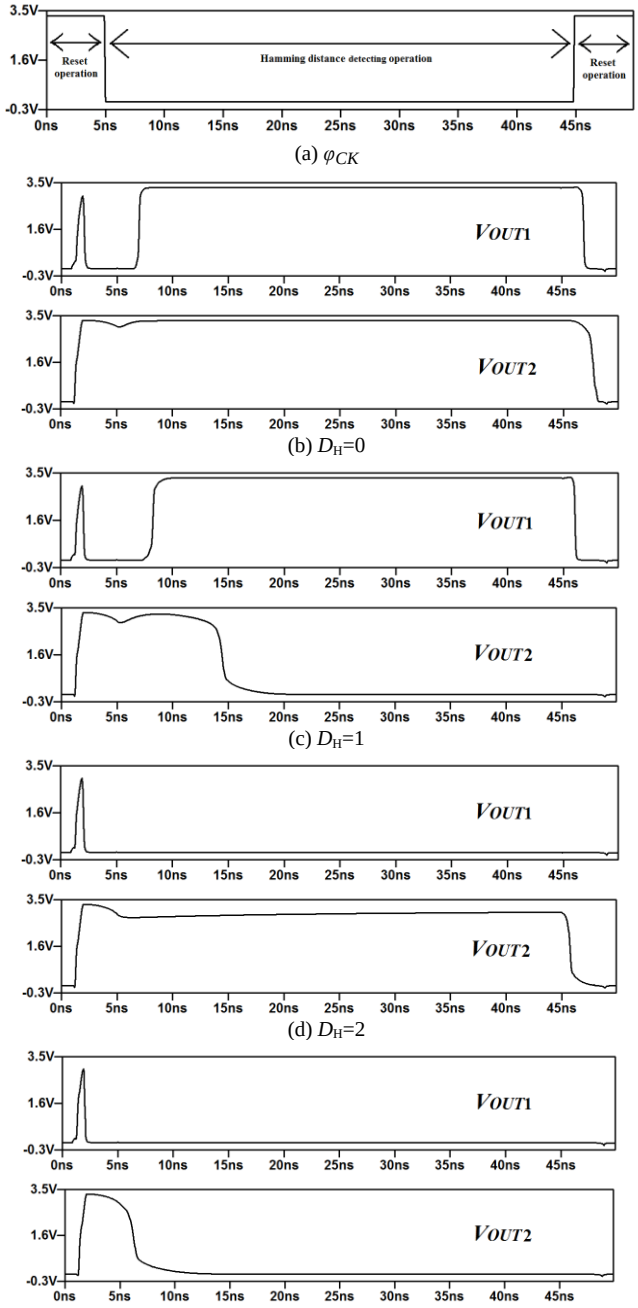
IV. SIMURATION WAVEFORMS

To verify the proposed detector, the computer simulations were carried out by LTspice.

Simulation waveforms are shown in Fig. 8. In this simulation, V_{DD} is taken 3.3(V), 0 of the Table II is taken 0(V) and 1 of the Table II is taken V_{DD}. Fig. 8(a) is the waveform of clock φ_{CK}. The operating states are divided by 2 states. These are reset operation when φ_{CK} is 3.3 (V), and Hamming distance detecting operation when φ_{CK} is 0(V). Fig. 8(b) is the waveforms when the Hamming distance D_H equals 0. As shown in Fig. 8 (b), V_{OUT1} outputs V_{DD} and V_{OUT2} outputs V_{DD} during the Hamming distance detecting operation. Fig. 8(c) is the waveforms when the D_H equals 1. As shown in Fig. 8(c), V_{OUT1} outputs V_{DD} and V_{OUT2} outputs 0(V) during the

Hamming distance detecting operation. Fig. 8 (d) is the waveforms when the Hamming distance D_H equals 2. As shown in Fig. 8(d), V_{OUT1} outputs 0(V) and V_{OUT2} outputs V_{DD} during the Hamming distance detecting operation. Fig. 8(e) is the waveforms when the D_H equals 3. As shown in Fig. 8(e), V_{OUT1} outputs 0(V) and V_{OUT2} outputs 0(V) during the Hamming distance detecting operation.

From these waveforms, this detector behaves properly as shown in Table II.



(a) φ_{CK}

(b) D_H=0

(c) D_H=1

(d) D_H=2

(e) D_H=3

Fig. 8. Simulation waveforms.

V. Conclusion

In this paper, we proposed the Hamming distance detector using a neuron CMOS A/D converter with 2 output terminals. This detector immediately detects Hamming distance between 2 input data. We verified that the proposed detector properly behaved by using LTspice. As shown in the simulation results, the detector has a delay from starting Hamming distance detecting operation to output the distance particularly in the circuit outputs 0(V). It is considered that the floating gate potential behaves around the inversion threshold voltage. One of the solutions of delay is using clock neuron CMOS inverter [6].

We consider that the proposed detector can be applied for pattern matching of antivirus system or dictionary search. In the future, the proposed detector may be applied to CAM.

Acknowledgment

The authors wish to thank to Mr. Yoshiki Sato for giving the advice of the proposed detector.

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