# 11-Bit 6.5MS/s SAR ADC for Wireless Applications

Saisundar. S, Simon Ng Sheung Yan, Huey Jen Lim, Bin Zhao, Dan Lei Yan, Minkyu Je, and Yoshida Akira

***Abstract*—A 1.3V, 11-bit, 6.5 MS/s Successive Approximation ADC is presented. The ADC operates with a differential peak to peak input of 1V. The ADC uses the common mode resetting triple level switching scheme, non-binary generalized redundant algorithm, a rail-to-rail latched comparator and a input bootstrapped sampling switch. The ADC was designed in 0.13um CMOS process. The simulation results of the ADC at an output data rate of 6.5 MS/s shows that it can achieve a signal-to-noise distortion ratio (SNDR) of 67.53 dB which corresponds to an Effective Number of Bits (ENOB) of 10.92. It also obtained a good linearity (DNL/INL) value of less than +-0.32LSB. The ADC consumes 414uW of power with a 1.3V supply resulting in a Figure of Merit (FOM) of 33 fJ/conversion-step.**

***Index Terms*—SAR ADC, triple level switching, non-binary, redundant algorithm.**

## I. Introduction

Electronic systems such as wireless transceivers, bio-implantable devices dictate stringent power consumption requirement. This requirement necessitates the development of low-power, low voltage systems that can take advantage of the technology scaling. Analog to digital convertors (ADC) are one of the key components in these devices for converting the analog quantities to digital data for information processing, data transmission and control. These applications need ADCs with moderate speed of few tens of MS/s and moderate resolution of 8-12 bits. There are various architectures that can be adopted for designing these ADCs. The pipeline ADC architecture is one of the commonly used architectures for wireless transceivers because of the high speed and better resolution that it can offer. These ADCs offer better power efficiency for moderate speeds, but the energy efficiency is still not low enough for micro power applications. The pipelined ADCs rely on op-amps to generate the residues and hence are not able to utilize the benefits of technology scaling. Successive Approximation Register analog to digital convertors (SAR ADC) have very good energy efficiency and are suitable for micro-power applications. The conversion time and power dissipation of SAR ADCs have become smaller with technology advancement [5].The resolution of the ADC was limited to about 8-10 bits because of the capacitor matching that can be obtained in the process. Designing a low power SAR ADC with medium resolution of 10-12 bits is a challenging task. The capacitor has to be sized such that it takes into account the kT/C noise which should be lesser than the quantization noise and also it should be sized such that it can have better matching. Various algorithmic techniques such as the non-binary algorithm, redundant algorithms with digital error correction have helped in achieving a higher ENOB number than that was obtained with the traditional designs [1]. With area efficient designs, low power consumption, moderate speed and resolutions of the order of 10 to 12 bits, the successive approximation ADCs have become a better alternative to the pipelined ADCs [5].

This paper proposes an 11-bit, 6.5MS/s differential input SAR ADC used for wireless applications. The ADC uses the generalized non-binary redundant algorithm to obtain better ENOB overcoming the process limits. It operates with a differential input of 1Vp-p and a supply voltage of 1.3V. A bootstrapped sampling switch is used to obtain higher linearity and faster settling at low supply voltages as compared to a transmission gate switch normally used in low-swing ADCs. The primary power dissipation components in SAR ADCs are the comparator and the reference voltage supplies used to charge and discharge the capacitors. This ADC uses a rail-to-rail latched comparator from the paper [3]. This comparator operates at high speed and has better linearity than the time domain comparator used in [4]. The SAR ADC uses the common-mode resetting triple level switching scheme presented in [4] to minimize the power consumption. The generalized non-binary redundant algorithm [1] reduces the effects of comparator errors due to mismatch and offset. It also minimizes the errors caused by mismatch of the capacitors and triple level switching.

## II. Architecture

The architecture of the SAR ADC is shown in Fig. 1. The SAR ADC consists of 7 major building blocks namely, bootstrapped sampling switch, capacitor array, switching array, rail-to-rail comparator, digital switching logic, redundant decoder and reset switching logic circuit.

### A. Bootstrapped Sampling Switch

The boot strapped switch [6]-[7] shown in Fig. 2 is used to sample the input on to the capacitor array. The sample and hold function is performed by the same capacitor array. The bootstrapped switch basically has a clock multiplier circuit that boosts the switching signal from 0-VDD to VDD-2VDD-ΔV. This signal is used to operate the input switch transistor. The switch maintains a constant VGS of VDD-ΔV

Manuscript received July 6, 2012; revised September 5, 2012.

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DOI: 10.7763/IJIEE.2012.V2.234

and hence provides a good linearity by maintaining a constant Ron of the MOSFET for the entire input range. The switch is sized based on the settling time required for the ADC.

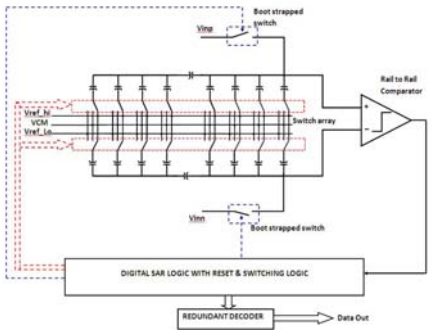


Fig. 1. Architecture of the proposed SAR ADC.

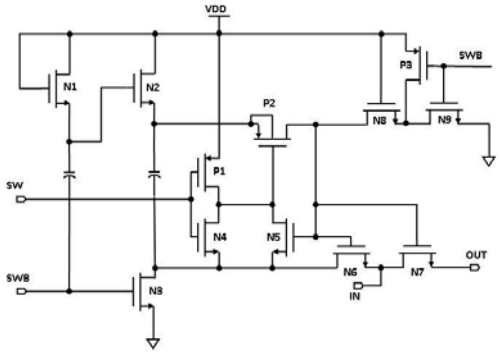


Fig. 2. Bootstrapped switch.

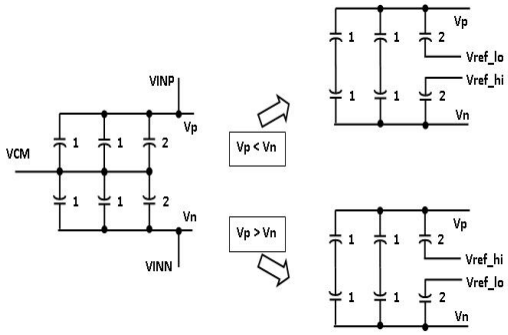


Fig. 3. Common mode resetting triple level switching scheme.

### B. Common Mode Resetting Triple Level Switching

The ADC uses the common mode resetting triple level switching as shown in Fig. 3[4]. During the sampling period the ADC capacitor array bottom plates are connected to VCM and the differential input is sampled on to the top plates of the capacitors. Based on the decision from the comparator, the bottom plate of the capacitor array will be switched to either Vref_hi or Vref_lo. Since the charging and discharging voltage swing is halved because of the use of third voltage level (VCM), the energy consumption will be 4 times lesser than the conventional method. The resetting is done by connecting the bottom plates of the two capacitor arrays together to VCM during the reset period.

### C. Capacitor Array and Redundant Code

The capacitor array was sized such that the kT/C noise is lesser than quantization noise of an 11 bit ADC. As per [8] the unit capacitor for an 11 bit ADC with a swing of 1Vp-p differential needs to be at least about 416fF.The process variation information for the capacitor matching set the minimum capacitor limit to 416fF to obtain an ENOB of at least 10.4. Hence a 416fF capacitor was used along with the non-binary redundant algorithm [1] to obtain a higher ENOB. This redundant algorithm introduces an additional bit in the conversion and hence an 11 bit ADC will take 12 cycles to perform a conversion. This additional bit helps in overcoming the errors that can happen due to incorrect DAC settling and comparator errors. The step size is non-binary and the redundant algorithm gives us a way to correct the errors of previous steps at the later steps. The algorithm relaxes the settling time of DAC and the capacitor. The settling time of the redundant SAR ADC can be expressed as [2].

$$Settling\ time = \tau \times \ln(p/q) \quad (1)$$

where p is the step size voltage change and q is the redundancy in that corresponding step and τ is the settling time of the capacitor array. This design used an 11 bit ADC with one redundant bit. The optimum sizing can be found by iterative simulation of the algorithm and the best sizing that gave a settling time of 2.4τ was found to be p(k)={1024,512,233,129,69,37,20,11,6,3,2,1}. To reduce the size of the capacitor array, a segmented capacitor array was utilized as shown in Fig. 1. An attenuation capacitor is inserted in between the MSB and LSB side of the array. Hence the size of the MSB capacitors can be reduced without changing the effective capacitor value. The sizing of the attenuation capacitor is based on [4].

### D. Comparator

A rail-to-rail latched comparator shown in Fig. 4 is used in the design. This comparator based on the design [3]. A 104MHz clock signal is used for the SAR ADC. The comparator has to be able to resolve faster than half of the clock cycle period (i.e 4.8ns). Hence low threshold transistors were used for the latch, digital gates and input transistor of the comparator whereas as normal threshold devices with longer lengths were used in the current mirrors. The comparator is sized such that it can operate with a resolution of 12 bits with a speed of less than 4.8ns.

### E. Digital SAR Logic and Switching Array

The switching arrays connected to the bottom plates of the capacitor arrays were implemented using MOSFET switches. These switches connect the bottom plates to the reference voltages. The SAR logic controls the switching activities of the switching arrays. Based on the decision of the previous bit, it switches the capacitor to either Vref_hi or Vref_lo. The digital SAR logic works at 104MHz and the logic generates the necessary timing signals and sampling signals internally. The SAR ADC takes 16 cycles to perform a conversion. The logic generates the sample signal that is used to sample the input on to the capacitor array in the first 3 cycles. The conversion starts from 4th cycle and takes 12 cycles to determine the 12-bit output. The last cycle is the used to latch the output and reset the capacitor array and then a new conversion cycle begins

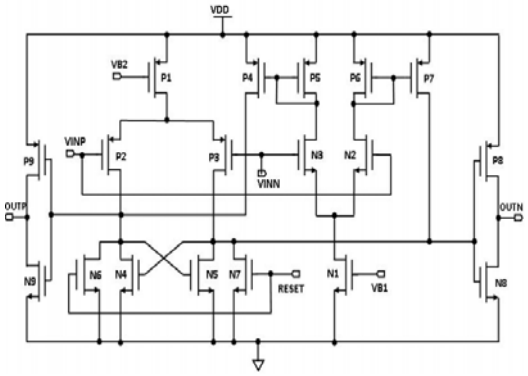


Fig. 4. Rail-to-rail latched comparator.

### F. Redundant Decoder

The output of the SAR ADC will be a 12 bit code, 11 bits with one redundant bit that is based on the non-binary sizing obtained from the steps mentioned in section C. To convert the output from 12-bit non-binary redundant code to an 11-bit binary non-redundant code (normal binary output), a redundant decoder was implemented. This decoder takes less than 1 ns to do the conversion and also provides a done signal that can be used for sampling the ADC output data.

## III. Simulation Results

The 11-bit 6.5MS/s dual channel successive approximation (SAR) analog-to-digital converter (ADC) for 1V peak to peak differential input was designed under 0.13um CMOS process. The layout of dual channel ADC test chip with input buffers is shown in Fig. 5.

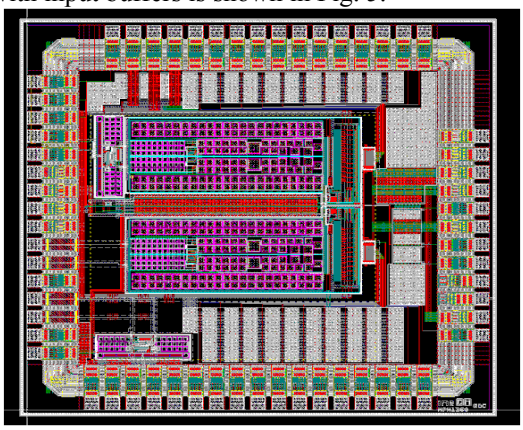

Fig. 5. Layout of the ADC test chip.

A single SAR ADC occupies an active area of 800um x 380um.The SAR ADC was simulated in various corners and temperatures and obtained an ENOB of greater than 10 and the DNL/INL of less than +-0.5 LSB. The simulation result of the ADC with a 1.2MHz, 1V peak to peak differential input signal at an output data rate of 6.5MS/s depicted in Fig. 6 showed that the ADC can achieve a SNDR of 67.53dB that corresponds to an ENOB of 10.92. The SFDR in various corners was also greater than 76.9 dBc. The DNL/INL simulations result illustrated in Fig. 7 showed that the ADC has a good linearity with the DNL less than +-0.18LSB and the INL less than +-0.32LSB. The ADC consumes 276uA of current from the 1.3V supply and 43uA each from the 0.9V high voltage reference and the low voltage reference of 0.4V.

The total power consumption of the ADC is 414uW.The FOM of the ADC derived based on the formula in (2) is about 33 fJ/conversion-step.

$$FOM = \frac{power}{2^{ENOB} \times fs} \quad (2)$$

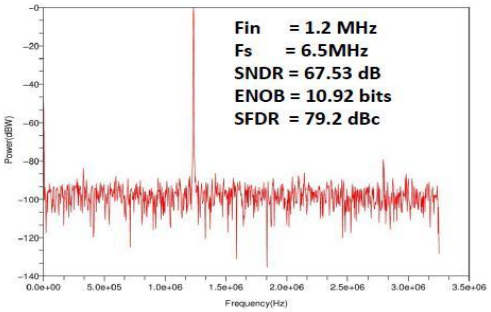


Fig. 6. Spectrum plot of the ADC.

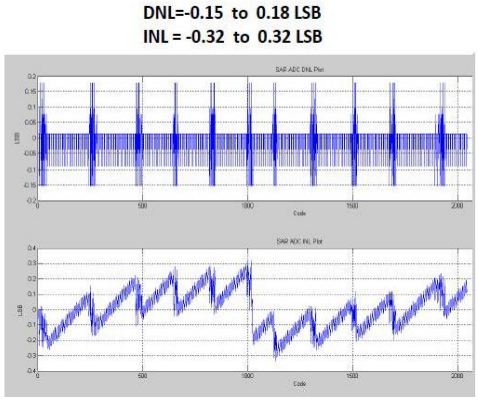


Fig. 7. Simulated DNL &INL plots of the ADC.

## IV. Conclusion

An 11-bit 6.5MS/s dual channel successive approximation (SAR) analog-to-digital converter (ADC) for a wireless transceiver application was designed under 0.13um CMOS process. The ADC achieved an ENOB of 10.92 consuming just 414uW of power with an FOM of 33fJ/conversion-step.

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