Modeling and Simulation of a CMOS-Based Analog Function Generator

Madina Hamiane

***Abstract*—Modeling and Simulation of an analog function generator is presented based on a polynomial expansion model .The proposed function generator model is based on a 10th order polynomial approximation of any of the required functions. The polynomial approximations of these functions can then be implemented using basic CMOS circuit blocks. In this paper, a circuit model is proposed that can simultaneously generate many different mathematical functions. The circuit model is designed and simulated with HSPICE and its performance is demonstrated through the simulation of a number of non-linear functions.**

***Index Terms*—Analog function generator, SPICE simulation, polynomial expansion modeling, CMOS HSPICE models.**

I. Introduction

Analog nonlinear circuits have many applications, especially in signal processing, communication, instrumentation, neural networks, and medical equipment. As a result , a large number of analog signal processors have been discussed in the literature. Initially, analog signal processors were designed with the use of passive electronic components such rersistors and simple semiconductor devices such as diodes and BJT transistors. With the advant of JFET and MOSFET transistors, the non-linear characteristics of these devices have then been exploited in the design of such processors. Many approaches involving the use of piecewise-linear function approximations of non-linear functions have been reported in the literature [1], [2]. In this respect, BJT and BiCMOS transistors have been used to simulate non-linear functions.

More recently, CMOS analog circuits based on the exponential-law and the square-law characteristics of a CMOS transistor operating in weak and strong inversion respectively have been reported [3], [4]. These circuit realizations present some disadvantages , the two most important being the realization of only one function at a time and their operation in voltage mode or mixed current and voltage mode. However, in current-mode circuits wider signal bandwidths and larger dynamic ranges of operation can be obtained as opposed to voltage-mode circuits.

A number of CMOS current-mode analog processors have been reported in the litearture. However, these circuits present many disadvantages such as their realization of only a few functions and only one funtion at a time [5]-[7]. In addition, these circuits are based on piecewise linear approximations of the non-linear functions.

A CMOS current-mode analog signal synthesizer has recently been proposed [7]. The circuit was based on a third order Taylor's series expansions of nonlinear functions which restricted the number of functions that can be realized and the accuracy of their realizations.

In this paper, a CMOS-based circuit model of a current-mode anlog function generator that can realize a large number of non-linear functions is presented . The circuit model is based on a 10^{th}-order polynomial approximation of any non-linear function and is compatible with the CMOS technology currently used in digital signal processing. Another adavantage of the proposed model is the operation of the CMOS transistors in the strong inversion region, leading to the possible circuit operation at high frequencies. Other advantages of the proposed circuit model are the simulatneous realization of many nonlinear functions at a time that do not need the use of piece linear approximation.

II. Proposed Circuit Model

In the proposed circuit model, a 10th order polynomial of the form is used to approximate non-linear functions with a high degree of accuracy. In current mode, with the variable x representing the normalized input current, equation (1) can be realized by taking the sum of the weighted output currents of a number of building blocks that consist of the traditional class-AB current mirror circuit to provide both power-raising and amplification of the current input, and adding it to a constant current.

$$f(x) = a_0 + a_1x + a_2x^2 + a_3x^3 + a_4x^4 + a_5x^5 + a_6x^6 + a_7x^7 + a_8x^8 + a_9x^9 + a_{10}x^{10}$$
$$|x| < 1 \quad (1)$$

One such building block is the squaring unit shown in Fig. 1 where I_{in} is the input current, I_b the bias current, and I_{out} is the output current. The aspect ratios (W/L) of transistors T_1 – T_8 of Fig. 1 are shown in Table I. The Transistors T_1 and T_2 as well as T_3 and T_4 are assumed to be well matched and transistors T_1 through T_8 are assumed to have the same value of the transconductance parameter i.e., $\beta n = \beta p$ and are operating in their saturation region. With these assumptions, the translinear principle is applied to produce the output current I_{out} which can be then expressed as [7].

$$I_{out} = \frac{I_{in}^2}{8I_b} \quad (2)$$

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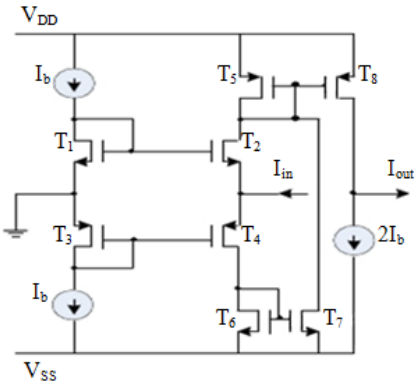

Fig. 1. Modified current mirror to provide output currents proportional to the square of the input current.

TABLE I: ASPECT RATIOS (W/L) FOR THE TRANSISTORS OF FIG. 1

Transistor	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8
W/L	1/ 1	1/ 1	1/ 1	1/ 1	1/ 1	1/ 1	1/ 1	1/ 1

In order to obatin another output current proportional to the input current, two additional transistors T_9 and T_{10} are added with aspect ratios 1/2 and 1/1 respectively as shown in Fig.2. From this circuit, output currents of value a_1x or a_2x^2 , can be obtained by using additional current mirrors of different aspect ratio values (W/L). By applying again the translinear principle , the output current I_1 is given by :

$$I_1 = -\frac{I_{in}}{2} \text{ or } \frac{I_1}{I_b} = -\frac{x}{2} \tag{3}$$

where $x = I_{in} / I_b$ represents the normalized input current.

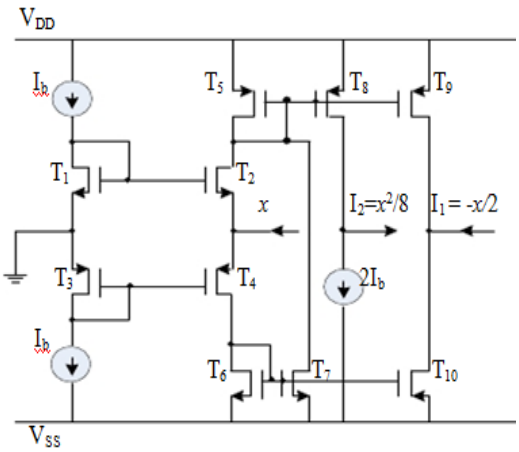

Fig. 2. Modified squaring circuit of Fig. 1 to provide output currents proportional to the input current and its square.

Equation (3) can also be re-written using the normalized input current as:

$$I_2 = \frac{I_{in}^{\,2}}{8I_b} \text{ or } \frac{I_2}{I_b} = \frac{x^2}{8} \tag{4}$$

In order to obtain a current proportional to x^3, the following relation is used:

$$\frac{(x+x^2)^2}{8} - \frac{(x-x^2)^2}{8} = \frac{x^3}{8} \tag{5}$$

The corresponding circuit will therefore requires two modified squaring circuits with inputs proportional to the difference and the sum of the input current and its square. The required third order term in (1) can then be obtained by selecting appropriate values of the aspect ratios (W/L). Therefore and in order to obtain output currents proportional to even and odd powers of the input current, the modified squaring circuit of Fig. 2 along with (4) and (5) are repeatedly used. TABLES II-A and II-B give the details of the inputs that are used to produce output currents proportional to x^3 through x^{10}.

TABLE II-A: OUTPUT CURRENTS PROPORTIONAL TO ODD POWERS OF INPUT CURRENTS

I_{in}	$x + x^2$ and $x - x^2$	$x + x^4$ and $x - x^4$	$x + x^6$ and $x - x^6$	$x + x^8$ and $x - x^8$
I_1	$x^3/2$	$x^5/2$	$x^7/2$	$x^9/2$

TABLE II-B: OUTPUT CURRENTS PROPORTIONAL TO EVEN POWERS OF INPUT CURRENTS

I_{in}	x	x^2	x^3	x^4	x^5
I_2	$x^2/8$	$x^4/8$	$x^6/8$	$x^8/8$	$x^{10}/8$

It can therefore be concluded that higher-order terms of equation (1) can be obtained by repetitive use of the circuit model of Fig. 2 without the need for dedicated current multipliers. With this design and the addition of a normalized DC current, any nonlinear function can be realized using MOSFET current-mirrors with the appropriate aspect ratios (W/L). Fig. 3 shows the basic circuit model of the function generator where B refers to the squaring circuit model of Fig. 2. The circuit shows only outputs proportional to x through x^6.

III. SIMULATION RESULTS

The basic circuit models of Fig. 3 was used in the simulation of a number of nonlinear functions. The corresponding polynomial expansion coefficients a_i, $i = 1, \ldots, 10$ for selected functions are given in Tables III-A and III-B, and the transistors' aspects ratios were selected accordingly. HSPICE circuit simulation environment was used and the simulation was carried out using the BSIM2 level 39 MOSFET transistor models with L=0.1μm, bias current I_b=1μA and supply voltages V_{DD} = -V_{SS} = 2V. For each function simulation, the input current was changed from 0 μA to 1μA, and the output currents through load resistances of 1=MΩ was obtained. A DC current source = 1μA was added to the output node to represent the constant term in equation (1) which equals, according to Tables III-A and III-B, either to 1 or zero.

The exact nonlinear functions were calculated and their graphs compared with those of the simulated functions as illustrated in Fig. 4 and Fig. 5. Inspection of these figures clearly shows that the simulated results are in excellent agreement with the calculated ones.

Table IV shows the range of input current values for which

the mean square error between corresponding functions is less than 1% which further reflects the accuracy of the proposed function generator circuit model.

TABLE III-A: POLYNOMIAL EXPANSION COEFFICIENTS FOR SELECTED FUNCTIONS

Function	a_0	a_1	a_2	a_3	a_4	a_5
sin(x)	0	1	0	-1/6	0	1/120
$\frac{1}{\sqrt{1+x}}$	1	-1/2	3/8	-5/16	35/ 128	- 0.2461
tanh(x)	0	1	0	-1/3	0	2/15
ln(1- x)	0	-1	-1/2	-1/3	-1/4	-1/5
e^x	1	1	1/2	1/6	1/24	1/120
$J_1(x)$	0	1/2	0	-1/16	0	1/384
$I_0(x)$	1	0	1/4	0	1/64	0
$\sqrt{1-x^2}$	1	0	-1/2	0	-1/8	0

TABLE III-B: POLYNOMIAL EXPANSION COEFFICIENTS FOR SELECTED FUNCTIONS

Function	a_6	a_7	a_8	a_9	a_{10}
sin(x)	0	-1/5040	0	1/362880	0
$\frac{1}{\sqrt{1+x}}$	0.2256	-0.2095	0.1964	-0.1855	0.1762
tanh (x)	0	-17/315	0	0.0219	0
ln(1-x)	-1/6	-1/7	-1/8	-1/9	-1/10
e^x	1/720	1/5040	1/40320	1/3628 8	1/3628
$J_1(x)$	0	-1/18432	0	1/14745	0
$I_0(x)$	1/2304	0	1/14745 6	0	1/147456
$\sqrt{1-x^2}$	-1/16	0	-5/128	0	-7/256

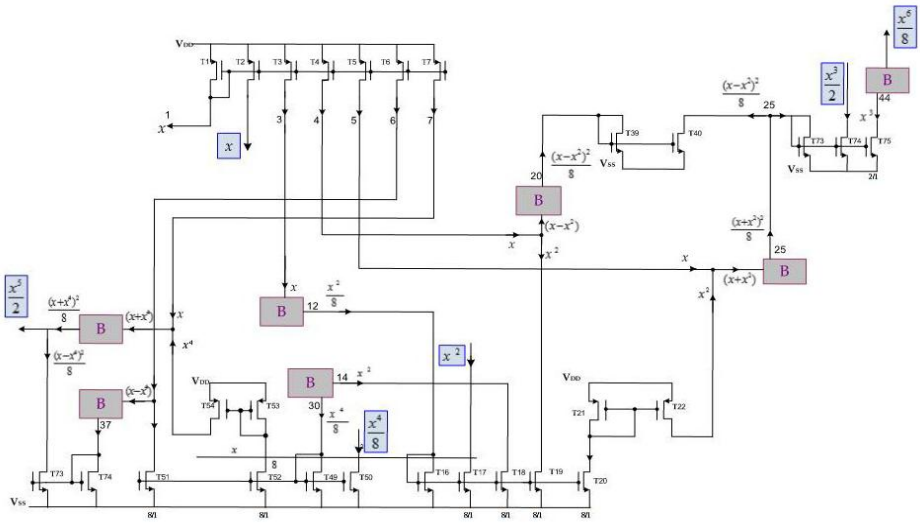

Fig. 3. Basic circuit model for the function generator showing outputs proportional to the first 6 terms of the polynomial expansion.

TABLE IV: RANGE OF INPUT CURRENT VALUES

Function	sin(x)	$\frac{1}{\sqrt{1+x}}$	tanh (x)	ln(1-x)
Range of x	< 1 μA	< 0.8 μA	< 1 μA	< 0.8 μA
Function	e^x	$J_1(x)$	$I_0(x)$	$\sqrt{1-x^2}$
Range of x	< 1 μA	< 1 μA	< 1 μA	< 0.9 μA

IV. CONCLUSION

Simulation of a simple function generator using MOSFET transistor models available in HSPICE simulation environment has been presented. The circuit model was based on approximating any nonlinear function with the first 10 terms in its polynomial expansion. The circuit model that realizes any of these functions consists of power-factor raising circuits built around a basic current squarer circuit, a weighted current amplifier and a dc current source. The proposed simulation model can be easily modified to implement many functions by proper selection of the transistors' aspect ratios. The accuracy of the synthesized function will be primarily decided by the number of terms used in the power expansion approximation and the effects of mismatch between transistors used in practical implementation of the required current-mirrors. Expanding further the approximation requires the use of additional similar power- raising circuit blocks. Simulation of a number of nonlinear functions supported by the evaluation of the mean square error between exact and simulated functions values verified the validity of the proposed function generator circuit model.

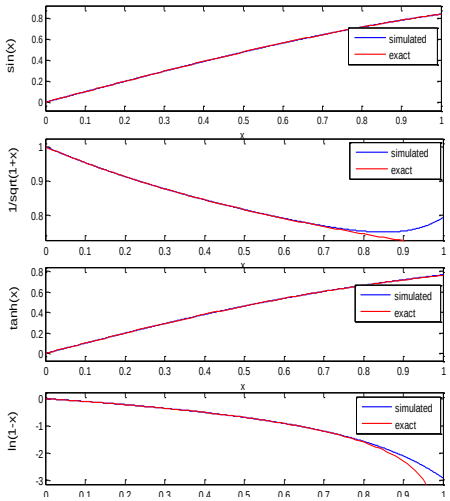

Fig. 4. Simulated and calculated functions from Table III-A and III-B.

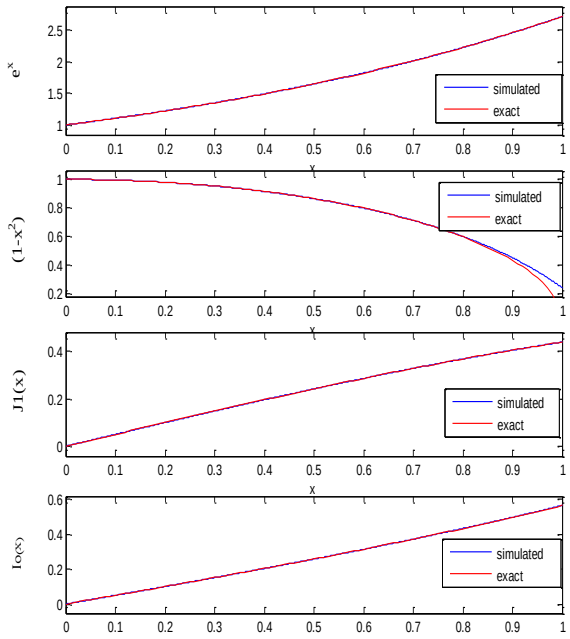

Fig. 5. Simulated and calculated functions from Table III-A and III-B.

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