Design of a Digitally Controlled Inductor-Less Voltage Multiplier for Non-Thermal Food Processing

Kei Eguchi, *Member, IACSIT*, Shinya Terada, and Ichirou Oota

***Abstract*—For non-thermal food processing systems utilizing an underwater shockwave, a digitally controlled voltage multiplier is proposed in this paper. The proposed voltage multiplier based on Cockcroft-Walton voltage multiplier (CWVM) has a bipolar structure. Unlike the conventional CWVM, the output voltage of the proposed multiplier is expressed by sum of the output voltage of positive and negative voltage multiplier blocks. Therefore, the number of stages of the proposed multiplier is about a half of that of the conventional CWVM. Furthermore, by utilizing high-low side drivers and a microcontroller, the diode switch of the proposed multiplier is driven by high-speed rectangular pulses. For these reasons, the proposed multiplier can achieve not only high voltage efficiency but also high speed operation. The validity of the circuit design is confirmed by theoretical analysis, simulation program with integrated circuit emphasis (SPICE) simulations, and experiments. The simulation results show that the settling time of the proposed voltage multiplier is less than 1/400 of that of the conventional CWVM. Furthermore, the experimental results show that the proposed voltage multiplier can improve voltage efficiency more than 21% from the conventional CWVM when the input voltage is 10V@60Hz and the output capacitor is 10μF.**

***Index Terms*—Cockcroft-Walton multipliers, high speed multipliers, non-thermal food processing, voltage multipliers.**

I. Introduction

Recently, a non-thermal food processing technology [1] has been widely studied to provide nutritious and fresh foods to consumers. The feature of the non-thermal food processing is that the destruction of nutrients and aroma by an increase of temperature is not caused with an increase in temperature. For this reason, several types of non-thermal food processing techniques have been proposed in past studies [1]: High Hydrostatic Pressure (HHP), Pulsed Electric Fields (PEF), High Voltage Arc Discharge (HVAD), Cold Plasma (CP), and so on [1]. Among others, we focused on the non-thermal technology utilizing an underwater shockwave [2]-[5] in this research. In the non-thermal food processing utilizing an underwater shockwave, the cell wall and organization of foods are destroyed by the high-speed destruction phenomenon that is called spalling destruction [2]-[5]. To achieve the spalling destruction, electrical energy stored in a capacitor is discharged and transferred into shockwave energy in a pressure vessel [3], [4]. For this reason, a high voltage multiplier to generate shockwave is one of the most important components in the non-thermal food processing utilizing an underwater shockwave.

In past studies, various types of high voltage multiplier have been proposed [6]-[11]. Among others, one of the most famous high voltage multipliers is the Cockcroft-Walton voltage multiplier (CWVM) [6]. Under no load condition, an N-stage (N=1, 2, …) CWVM can provide a DC voltage with the value of $2N$ times of the magnitude of the AC input source. The feature of the CWVM is that the CWVM can eliminate the requirement for the heavy core compared with a high voltage transformer with high turn ratio. For this reason, the CWVM has been continuously improved by many researchers. For example, Wang et al exhibited a cascade CWVM and its model of parasitic capacitances. However, it requires a transformer with center-tapped secondary to perform its push-pull kind of operation. To solve this problem, Iqbal proposed a symmetrical CWVM using a cascade rectifier circuit [8]. By cascading a diode-bridge rectifier, the CWVM in [8] requires only one secondary winding of the transformer. However, due to the electrical impedance of capacitors in lower stages, the output voltage of the voltage multipliers in [7] and [8] begins to sag according to the increase of the number of stages. Therefore, the voltage efficiency is lowered in the case of high conversion ratios. To generate a high voltage by the CWVM with a small number of stages, Young et al proposed a boost type voltage multiplier based on the CWVM [9], [10]. By combining a boost converter and a CWVM, the voltage multipliers in [9] and [10] generate a high voltage with a small number of stages. However, the voltage multipliers in [9] and [10] require a large inductor. Furthermore, the speed of these conventional CWVMs is slow, because the diode switch is controlled by a sinusoidal waveform supplied by a commercial power source. In the non-thermal food processing utilizing an underwater shockwave, it is necessary to generate a large shockwave many times to crush hard food. For this reason, the voltage multiplier which exhibits high response speed is required. Of course, high speed operation can be achieved by driving the CWVM from a combination of an inverter and a high voltage transformer. However, it becomes heavy owing to the high voltage transformer.

In this paper, a digitally controlled voltage multiplier is proposed for non-thermal food processing systems utilizing an underwater shockwave. The proposed voltage multiplier based on the CWVM can be designed without magnetic components. Unlike the conventional CWVMs generating a

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positive output voltage [6]-[10], the proposed voltage multiplier is formed by combining positive and negative voltage multiplier blocks. Namely, the proposed voltage multiplier has a bipolar structure. Of course, Patel et al. proposed a negative CWVM [11] in past studies. However, the voltage multiplier in [11] also has the problem in circuit speed and voltage efficiency. In the proposed voltage multiplier, the output voltage is expressed by sum of the output voltage of $2N+1$ (N=1, 2, …) times positive multiplier and $-2N$ times negative multiplier. Owing to the bipolar structure, the number of stages of the proposed voltage multiplier is about a half of that of the conventional CWVM. Therefore, the proposed voltage multiplier can alleviate the sag of the output voltage. Furthermore, by utilizing high-low side drivers and a microcontroller, the diode switch of the proposed voltage multiplier is driven by high-speed rectangular pulses. Therefore, the proposed voltage multiplier can achieve high speed operation. To confirm the validity of the proposed voltage multiplier, theoretical analysis, simulation program with integrated circuit emphasis (SPICE) simulations and experiments are performed.

II. System Architecture

Fig. 1 shows the system architecture of the non-thermal food processing systems utilizing an underwater shockwave. The operation of Fig. 1 is as follows: First, a high voltage is generated by a high voltage multiplier, where the target output voltage of our system is about 3.5kV. Next, electrical energy stored in a capacitor of the high voltage multiplier is discharged and transferred into shockwave energy in the pressure vessel. Then a shockwave propagates in water to crush foods. Finally, the target food is destroyed by spalling destruction.

In past studies, the design of the pressure vessel was discussed in [3] and [4]. Furthermore, the characteristic of the underwater shockwave was reported in [2]. For this reason, we discuss the design of the high voltage multiplier to generate an underwater shockwave in this paper.

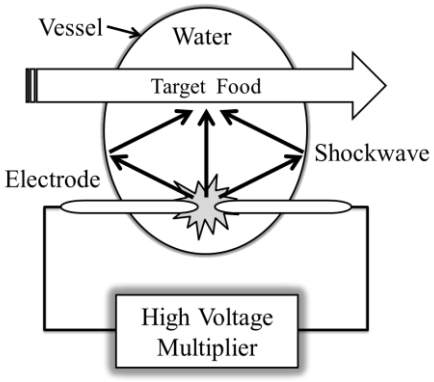


Fig. 1. System architecture of the non-thermal food processing system utilizing an underwater shockwave.

III. Circuit Structure

A. Conventional Multiplier

Fig. 2 shows the conventional Cockcroft-Walton voltage multiplier [6] with N stages (N=1, 2, …). By switching diodes, the conventional voltage multiplier generates the following output voltage:

$$V_{out} \cong 2N\left(V_{in} - V_{th}\right). \tag{1}$$

In (1), V_{in} is the maximum value of an AC input voltage and V_{th} is the threshold voltage of the diode switch. As Fig. 2 shows, the conventional voltage multiplier can realize the simple circuit constitution. However, the speed of the conventional multiplier is slow, because the diode switch is controlled by a sinusoidal waveform supplied by a commercial power source. Concretely, the voltage V_{in} in Japan is 100V and the frequency of electric current is 50 Hz in Eastern Japan and 60 Hz in Western Japan.

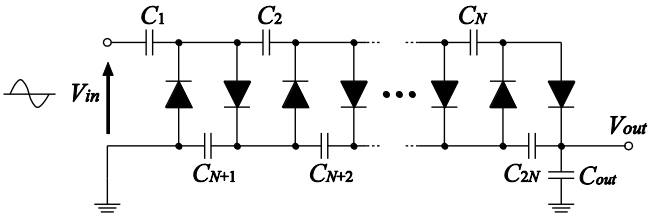


Fig. 2. Conventional voltage multiplier.

B. Proposed Multiplier

Fig. 3 shows the block diagram of the proposed voltage multiplier. The proposed voltage multiplier consists of a full waveform rectifier, a clock pulse generator, and a bipolar voltage multiplier. The operation of Fig. 3 is as follows: First, the AC signal V_{AC} is full-wave rectified by a full-wave rectifier. Then, the non-overlapped two-phase clock pulses Φ_1 and Φ_2 are generated by using the full-wave rectified voltage V_{cc}. Finally, the input V_{cc} is stepped up by the bipolar voltage multiplier.

Fig. 4 shows the proposed bipolar voltage multiplier. The proposed voltage multiplier consists of two voltage multiplier blocks: a positive voltage multiplier and a negative voltage multiplier. The proposed voltage multiplier generates the following stepped-up voltage:

$$\begin{aligned} V_{out} &= V_{po} - V_{mo}, \\ &\cong \left(4N+1\right)V_{in} - 2\left(2N+1\right)V_{th}, \end{aligned} \tag{2}$$

where

$$V_{po} \cong \left(2N+1\right)V_{cc} - \left(2N+1\right)V_{th}$$

and

$$V_{mo} \cong -2NV_{cc} + \left(2N+1\right)V_{th}.$$

As (2) shows, the output voltage V_{out} across the output capacitor is expressed by sum of the output voltage of positive voltage multiplier (V_{po}) and negative voltage multiplier (V_{mo}). Therefore, the number of stages of the proposed multiplier is about a half of that of the conventional voltage multiplier. Concretely, in the proposed voltage multiplier, the parameter N is set to seven to generate an output voltage more than 3.5kV. On the other hand, the parameter N is set to fourteen in the conventional voltage multiplier. Therefore, the proposed voltage multiplier can alleviate the sag of the output voltage. In other word, the

proposed voltage multiplier can achieve high voltage efficiency. Moreover, by utilizing high-low side drivers and a microcontroller, high-speed clock pulses Φ_1 and Φ_2 are generated to drive diode switches. Therefore, the proposed multiplier can achieve high speed operation without magnetic components.

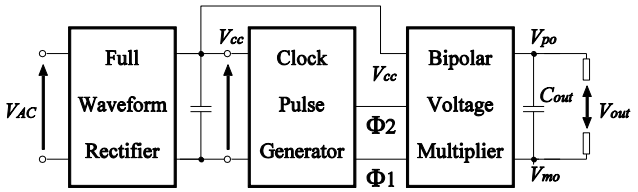


Fig. 3. Block diagram of the proposed voltage multiplier.

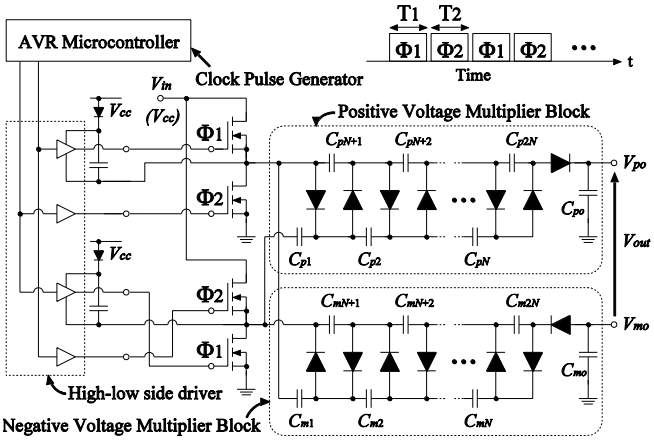


Fig. 4. Proposed bipolar voltage multiplier using a digital controller.

IV. Theoretical Analysis

In this section, the property of the proposed voltage multiplier is analyzed theoretically. In the theoretical analysis, we assume that 1) Parasitic elements are negligibly small and 2) Time constant is much larger than the period of clock pulses.

Fig. 5 shows the instantaneous equivalent circuits of the proposed voltage multiplier, where 1) Transistor switch is modeled by an ideal switch with the on-resistance R_{on} and 2) Diode switch is modeled by a voltage source V_{th} and an ideal switch with the on-resistance R_d. In the steady state, the differential value of electric charges in C_{pk} and C_{mk} satisfies the following equations:

$$\Delta q_{T_1}^{pk} + \Delta q_{T_2}^{pk} = 0 \tag{3}$$

and

$$\Delta q_{T_1}^{mk} + \Delta q_{T_2}^{mk} = 0,$$

where Δq_{Ti}^{mk} and Δq_{Ti}^{pk} ($(i=1, 2)$ and $(k=1,2, \ldots, 2N)$) denote the electric charges of the k-th capacitor in the case of State-T_i. The interval of State-T_i satisfies the following conditions:

$$T = T_1 + T_2,\ T_1 = DT,\ \text{and}\ T_2 = (1-D)T, \tag{4}$$

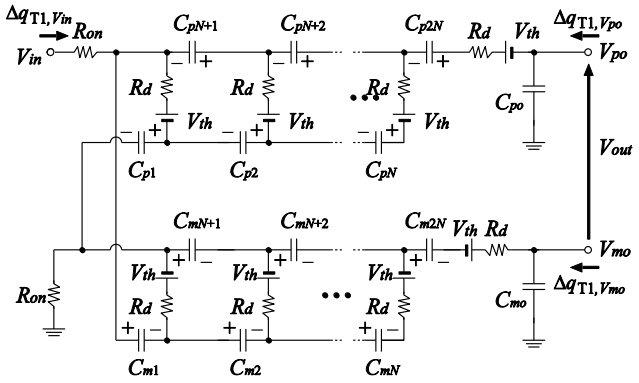
where T is the period of clock pulses, T_i (i=1, 2) is the pulse width of Φ_i, and D denotes the duty factor. In State-T_1, the differential values of electric charges in V_{in}, V_{po}, and V_{mo}, $\Delta q_{T1,Vin}$, $\Delta q_{T1,Vpo}$, and $\Delta q_{T1,Vmo}$, are expressed by

$$\Delta q_{T_1,V_{in}} = \Delta q_{T_1}^{p1} - \Delta q_{T_1}^{p2} - \Delta q_{T_1}^{pN+1} + \Delta q_{T_1}^{m1}, \tag{5}$$

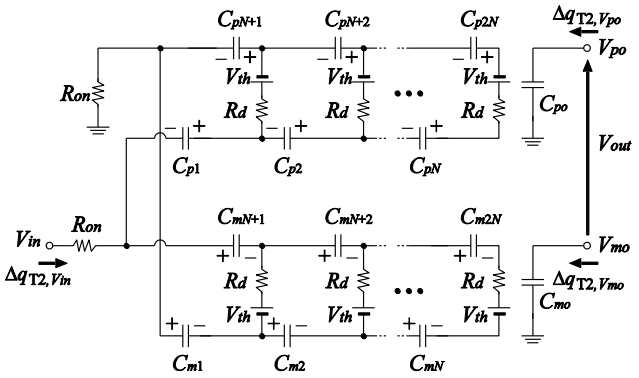
$$\Delta q_{T_1,V_{po}} = \Delta q_{T_1}^{p2N} + \Delta q_{T_1}^{po},$$

and

$$\Delta q_{T_1,V_{mo}} = -\Delta q_{T_1}^{m2N} - \Delta q_{T_1}^{mo}.$$



(a)



(b)

Fig. 5. Instantaneous equivalent circuits of the proposed bipolar voltage multiplier. (a) State-T_1, (b) State-T_2.

On the other hand, in State-T_2, the differential values of electric charges in V_{in}, V_{po}, and V_{mo}, $\Delta q_{T2,Vin}$, $\Delta q_{T2,Vpo}$, and $\Delta q_{T2,Vmo}$, are expressed by

$$\Delta q_{T_2,V_{in}} = -\Delta q_{T_2}^{p1} + \Delta q_{T_2}^{mN+1}, \tag{6}$$

$$\Delta q_{T_2,V_{po}} = \Delta q_{T_2}^{po},$$

and

$$\Delta q_{T_2,V_{mo}} = -\Delta q_{T_2}^{mo}.$$

Using (5) and (6), the average input current and the average output current can be expressed as

$$\overline{I_{in}} = \frac{\Delta q_{V_{in}}}{T} = \frac{\Delta q_{T_1,V_{in}} + \Delta q_{T_2,V_{in}}}{T}, \tag{7}$$

$$\overline{I_{po}} = \frac{\Delta q_{V_{po}}}{T} = \frac{\Delta q_{T_1,V_{po}} + \Delta q_{T_2,V_{po}}}{T},$$

and

$$\overline{I_{mo}} = \frac{\Delta q_{V_{mo}}}{T} = \frac{\Delta q_{T_1,V_{mo}} + \Delta q_{T_2,V_{mo}}}{T},$$

where

$$\Delta q_{V_o} = \Delta q_{V_{po}} = -\Delta q_{V_{mo}}. \tag{8}$$

In (7), Δq_{Vin}, Δq_{Vpo}, and Δq_{Vmo} are electric charges in V_{in}, V_{po}, and V_{mo}, respectively. Substituting (3)-(6) into (7), we have the relation between the average input current and the average output currents as follows:

$$\overline{I_{in}} = -(2N+1)\overline{I_{po}} + (2N)\overline{I_{mo}}, \tag{9}$$

where

$$\Delta q_{V_{po}} = -\left(\frac{1}{N}\right)\Delta q_{T_1}^{p1}$$

and

$$\Delta q_{V_{mo}} = \left(\frac{1}{N}\right)\Delta q_{T_1}^{m1}. \tag{10}$$

Next, let us consider the consumed energy in one period. Using (3)-(10), the consumed energy W_T can be expressed as

$$W_T = W_{T_1} + W_{T_2}, \tag{11}$$

$$= 2(N+1)\frac{(\Delta q_{V_o})^2}{DT}R_d + 2(2N+1)^2\frac{(\Delta q_{V_o})^2}{DT}R_{on} + 2N\frac{(\Delta q_{V_o})^2}{(1-D)T}R_d + 8N^2\frac{(\Delta q_{V_o})^2}{(1-D)T}R_{on}$$

where

$$W_{T_1} = \frac{(\Delta q_{T_1}^{p1} - \Delta q_{T_1}^{p2})^2}{T_1}R_d + \cdots + \frac{(\Delta q_{T_1}^{pN-1} - \Delta q_{T_1}^{pN})^2}{T_1}R_d + \frac{(\Delta q_{T_1}^{pN})^2}{T_1}R_d + \frac{(\Delta q_{T_1}^{p2N})^2}{T_1}R_d + \frac{(\Delta q_{T_1}^{pN+1} + \Delta q_{T_1}^{p2} - \Delta q_{T_1}^{p1} - \Delta q_{T_1}^{m1})^2}{T_1}R_{on} + \frac{(\Delta q_{T_1}^{m1} - \Delta q_{T_1}^{m2})^2}{T_1}R_d + \cdots + \frac{(\Delta q_{T_1}^{mN-1} - \Delta q_{T_1}^{mN})^2}{T_1}R_d + \frac{(\Delta q_{T_1}^{mN})^2}{T_1}R_d + \frac{(\Delta q_{T_1}^{m2N})^2}{T_1}R_d + \frac{(\Delta q_{T_1}^{mN+1} + \Delta q_{T_1}^{m2} - \Delta q_{T_1}^{m1} - \Delta q_{T_1}^{p1})^2}{T_1}R_{on}$$

and

$$W_{T_2} = \frac{(\Delta q_{T_2}^{p1} - \Delta q_{T_2}^{p2})^2}{T_2}R_d + \cdots + \frac{(\Delta q_{T_2}^{pN-1} - \Delta q_{T_2}^{pN})^2}{T_2}R_d + \frac{(\Delta q_{T_2}^{m1} - \Delta q_{T_2}^{m2})^2}{T_2}R_d + \cdots + \frac{(\Delta q_{T_2}^{mN-1} - \Delta q_{T_2}^{mN})^2}{T_2}R_d + \frac{(\Delta q_{T_2}^{pN})^2}{T_2}R_d + \frac{(\Delta q_{T_2}^{mN})^2}{T_2}R_d + \frac{(\Delta q_{T_2}^{m1} - \Delta q_{T_2}^{pN+1})^2}{T_2}R_{on} + \frac{(\Delta q_{T_2}^{p1} - \Delta q_{T_2}^{mN+1})^2}{T_2}R_{on}.$$

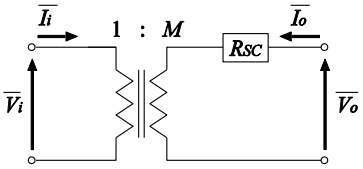


Fig. 6. General equivalent circuit of capacitor-based converters.

Here, it is known that a general equivalent circuit of capacitor-based converters can be expressed by the circuit shown in Fig. 6 [12], [13], where R_{SC} is called the SC resistance and M is the ratio of an ideal transformer. In the general equivalent circuit of capacitor-based converters, the consumed energy can be defined as

$$W_T := \left(\frac{\Delta q_{V_o}}{T}\right)^2 \cdot R_{SC} \cdot T \cdot \tag{12}$$

Substituting (11) into (12), the SC resistance of the bipolar voltage multiplier can be obtained as

$$R_{SC} = \frac{\{2(N+1)(1-D)+2ND\}}{D(1-D)}R_d + \frac{\{2(2N+1)^2(1-D)+8N^2D\}}{D(1-D)}R_{on}. \tag{13}$$

In (13), the SC resistance R_{SC} becomes a minimum value when

$$\frac{dR_{SC}}{dD} = 0 \quad \text{and} \quad 0 < D < 1. \tag{14}$$

From (13) and (14), the optimal duty factor to achieve the minimum R_{SC} is obtained as

$$D = \alpha - \sqrt{\alpha(\alpha-1)}, \tag{15}$$

where

$$\alpha = \frac{(N+1)R_d + (2N+1)^2 R_{on}}{R_d + (4N+1)R_{on}}. \tag{16}$$

By combining (9) and (13), we have the equivalent circuit of the proposed bipolar voltage multiplier as follows:

$$\begin{bmatrix} \overline{V_{in}} - \dfrac{2(2N+1)}{4N+1}V_{th} \\ \overline{I_{in}} \end{bmatrix} = \begin{bmatrix} \dfrac{1}{4N+1} & 0 \\ 0 & 4N+1 \end{bmatrix} \begin{bmatrix} 1 & R_{SC} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \overline{V_{out}} \\ -\overline{I_{out}} \end{bmatrix}, \tag{17}$$

Because the equivalent circuit can be expressed by a Kettenmatrix (see Fig. 6). Using (13) and (17), the equivalent circuit of the bipolar voltage multiplier can be expressed by Fig. 7. When the output load is the resistive load R_L, the power efficiency η and the output voltage V_{out} are obtained as

$$\eta = \frac{R_L}{R_L + R_{SC}} \left\{ \frac{(4N+1)\overline{V_{in}} - 2(2N+1)V_{th}}{(4N+1)\overline{V_{in}}} \right\} \quad (18)$$

and

$$\overline{V_{out}} = \frac{R_L}{R_L + R_{SC}} \left\{ (4N+1)\overline{V_{in}} - 2(2N+1)V_{th} \right\}. \quad (19)$$

In the same way, the property of the conventional CWVM can be analyzed theoretically. The theoretical analysis concerning the conventional CWVM will be described in Appendix.

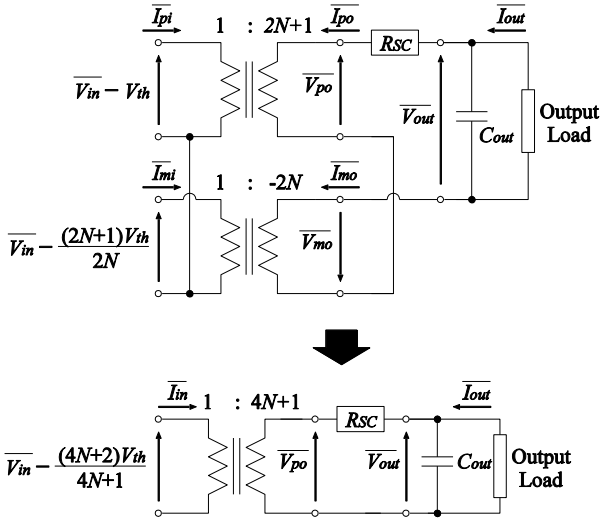


Fig. 7. Equivalent circuit of the proposed bipolar voltage multiplier.

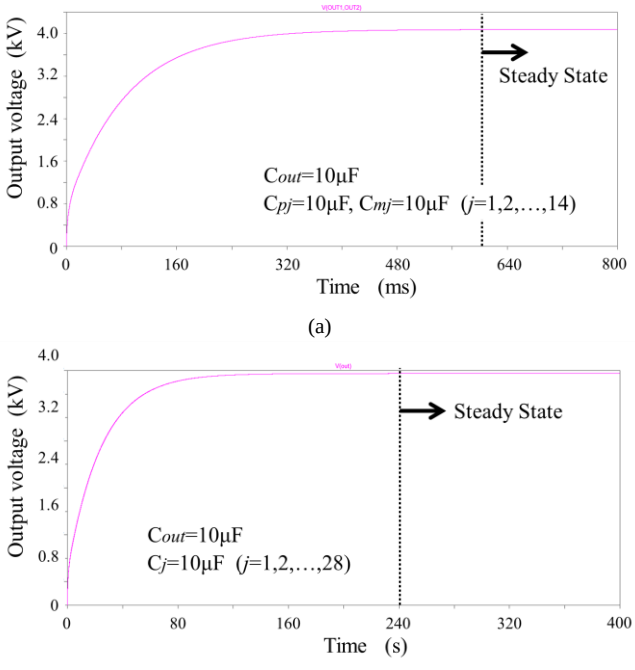


Fig. 8. Instantaneous equivalent circuits of the voltage multiplier. (a) Proposed voltage multiplier, (b) Conventional voltage multiplier.

V. Simulation

To clarify circuit characteristics, SPICE simulations are performed concerning the proposed voltage multiplier with seven stages (N=7) and the conventional CWVM with fourteen stages (N=14). The conditions for the SPICE simulation are as follows: V_{AC}= 100V@60Hz, T= 100μs, and C_{out}= 10μF.

Fig. 8 (a) shows the simulated output of the proposed voltage multiplier and Fig. 8 (b) shows the simulated output of the conventional CWVM shown in Fig. 2. As Fig. 8 (a) shows, the proposed voltage multiplier can generate more than 3.5kV at high speed. Concretely, the settling time of the proposed voltage multiplier is less than 600ms when the capacitors C_{pi} and C_{mi} (i=1, 2, …, 14) are 10μF.

On the other hand, the settling time of the conventional CWVM is about 240 seconds when the capacitors C_j (j=1, 2, …, 28) are 10μF. In other words, the settling time of the proposed voltage multiplier is less than 1/400 of that of the conventional multiplier. As these results show, the proposed voltage multiplier can achieve high speed operation.

VI. Experiment

To confirm the validity of the circuit topology, experimental circuit was built with commercially available components on a breadboard. Fig. 9 shows the laboratory prototype of the proposed voltage multiplier. In the experiment, the proposed voltage multiplier with seven stages (N=7) was assembled with diode switch 1N4007, high-low side driver IR2110PBF, MOSFET 2SK2382, electrolytic capacitor 10μF, bridge diode S1NB60, and microcontroller ATMEGA88- 20PU.

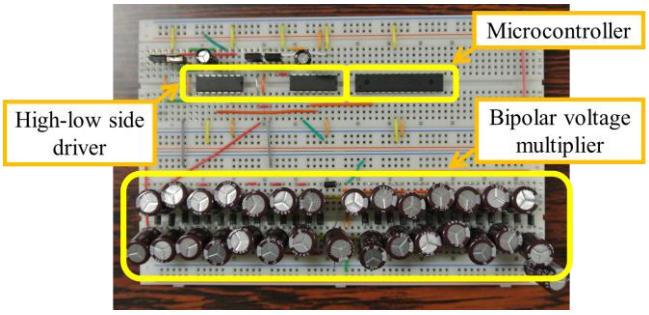


Fig. 9. Experimental circuit of the proposed voltage multiplier.

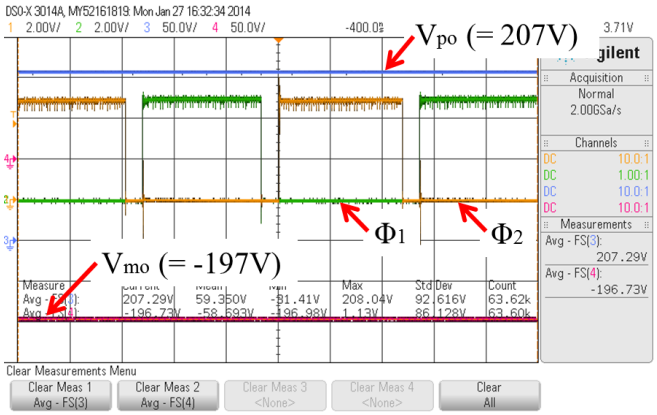


Fig. 10. Measured output voltage of the proposed voltage multiplier.

Fig. 10 shows the measured output voltage of the proposed voltage multiplier and Fig. 11 shows the measured output voltage of the conventional CWVM. In Fig. 10 and Fig. 11, the experiments were performed under conditions that the input voltage V_{AC} is 10V@60Hz and clock frequency of Φ_1 and Φ_2 is 10kHz, because we do not have a high voltage

probe. In Fig. 10, the measured output voltage of the proposed voltage multiplier is 404V (= 207+197 V). The voltage efficiency of the proposed voltage multiplier is 98.8%, because the ideal output voltage is 409V (= 29 ×14.1 V). The validity of the circuit topology can be confirmed by Fig. 10. On the other hand, the measured output voltage of the conventional CWVM is 307V. The voltage efficiency of the conventional CWVM is 77.7%, because the ideal output voltage is 395V (= 28 ×14.1 V). As Fig. 10 and Fig. 11 show, the proposed voltage multiplier can improve voltage efficiency more than 21% from the conventional CWVM.

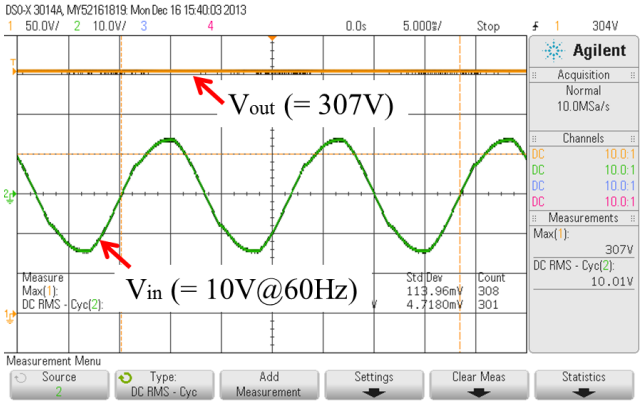


Fig. 11. Measured output voltage of the conventional CWVM.

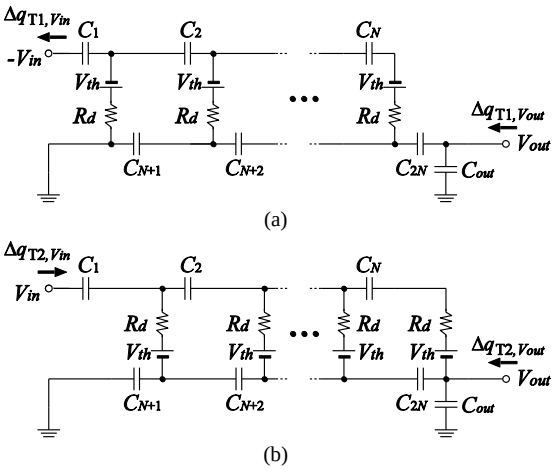


Fig. 12. Instantaneous equivalent circuits of the conventional CWVM. (a) State-T_1, (b) State-T_2.

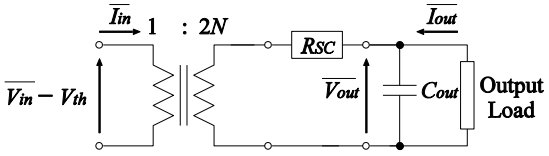


Fig. 13. Equivalent circuit of the conventional CWVM.

VII. Conclusion

For non-thermal food processing systems utilizing an underwater shockwave, a high-speed bipolar voltage multiplier has been proposed in this paper. The validity of circuit design was confirmed by theoretical analysis, SPICE simulations, and experiments.

The result of SPICE simulations showed that the proposed voltage multiplier can achieve higher speed operation than the conventional CWVM. Concretely, the settling time of the proposed voltage multiplier with seven stages is less than 600ms when the capacitor values are 10μF. On the other hand, the settling time of the conventional CWVM with fourteen stages is about 240 seconds when the capacitor values are 10μF. Namely, the settling time of the proposed voltage multiplier is less than 1/400 of that of the conventional multiplier.

Furthermore, the results of the laboratory experiment showed that the proposed voltage multiplier can realize higher voltage efficiency than the conventional CWVM. Concretely, the voltage efficiency of the proposed voltage multiplier is 98.8%. On the other hand, the voltage efficiency of the conventional CWVM is 77.7%. Namely, the proposed voltage multiplier can improve voltage efficiency more than 21% from the conventional CWVM.

The proposed voltage multiplier will enable high-speed operation of the non-thermal food processing system utilizing an underwater shockwave. The experimental evaluation of the non-thermal food processing system using the proposed voltage multiplier is left to a future study.

Appendix

In this section, the property of the conventional CWVM of Fig. 2 is analyzed theoretically. To simplify the theoretical analysis, we assume that the AC input voltage is a rectangular pulse whose amplitude is V_{in}.

Fig. 12 shows the instantaneous equivalent circuits of the conventional CWVM, where the diode switch is modeled by a voltage source V_{th} and an ideal switch with the on-resistance R_d.

$$\Delta q_{T_1}^{k} + \Delta q_{T_2}^{k} = 0 \tag{20}$$

where $\Delta q_{Ti}^{\ k}$ ((i=1, 2) and (k=1,2, …, 2N)) denotes the electric charge of the k-th capacitor in the case of State-T_i. The interval of State-T_i satisfies the condition of (4). In State-T_1, the differential values of electric charges in V_{in} and V_{out}, $\Delta q_{T1,Vin}$ and $\Delta q_{T1,Vout}$, are expressed by

$$\Delta q_{T_1,V_{in}} = -\Delta q_{T_1}^{1} \tag{21}$$

and $$\Delta q_{T_1,V_{out}} = \Delta q_{T_1}^{2N} + \Delta q_{T_1}^{out}$$

On the other hand, in State-T_2, the differential values of electric charges in V_{in} and V_{out}, $\Delta q_{T2,Vin}$ and $\Delta q_{T2,Vout}$,, are expressed by

$$\Delta q_{T_2,V_{in}} = -\Delta q_{T_2}^{1} \tag{22}$$

and $$\Delta q_{T_2,V_{out}} = \Delta q_{T_2}^{N} + \Delta q_{T_2}^{2N} + \Delta q_{T_2}^{out}.$$

using (21) and (22), the average input current and the average output current can be expressed as

$$\overline{I_{in}} = \frac{\Delta q_{V_{in}}}{T} = \frac{-\Delta q_{T_1,V_{in}} + \Delta q_{T_2,V_{in}}}{T}, \tag{23}$$

and $$\overline{I_{out}} = \frac{\Delta q_{V_{out}}}{T} = \frac{\Delta q_{T_1,V_{out}} + \Delta q_{T_2,V_{out}}}{T}.$$

In (23), Δq_{Vin} and Δq_{Vout} are electric charges in V_{in} and V_{out}, respectively. Substituting (20)-(22) into (23), we have the relation between the average input current and the average output current as follows:

$$\overline{I_{in}} = -(2N)\overline{I_{out}}, \tag{24}$$

where

$$\Delta q_{V_{out}} = -\left(\frac{1}{N}\right)\Delta q_{T_1}^1. \tag{25}$$

Next, let us consider the consumed energy in one period. Using (20)-(25), the consumed energy W_T can be expressed as

$$W_T = W_{T_1} + W_{T_2} \tag{26}$$

$$= N\frac{\left(\Delta q_{V_{out}}\right)^2}{DT}R_d + N\frac{\left(\Delta q_{V_{out}}\right)^2}{(1-D)T}R_d,$$

where

$$W_{T_1} = \frac{\left(\Delta q_{T_1}^1 - \Delta q_{T_1}^2\right)^2}{T_1}R_d + \cdots + \frac{\left(\Delta q_{T_1}^{N-1} - \Delta q_{T_1}^N\right)^2}{T_1}R_d + \frac{\left(\Delta q_{T_1}^N\right)^2}{T_1}R_d$$

and

$$W_{T_2} = \frac{\left(\Delta q_{T_2}^1 - \Delta q_{T_2}^2\right)^2}{T_2}R_d + \cdots + \frac{\left(\Delta q_{T_2}^{N-1} - \Delta q_{T_2}^N\right)^2}{T_2}R_d + \frac{\left(\Delta q_{T_2}^N\right)^2}{T_2}R_d$$

From Fig. 6, the consumed energy of a general capacitor-based converter can be expressed as

$$W_T := \left(\frac{\Delta q_{V_o}}{T}\right)^2 \cdot R_{SC} \cdot T \cdot \tag{27}$$

Therefore, by substituting (26) into (27), the SC resistance of the conventional CWVM can be obtained as

$$R_{SC} = \frac{N}{D(1-D)}R_d \cdot \tag{28}$$

From (14) and (28), the optimal duty factor to achieve the minimum R_{SC} is obtained by D=0.5. By combining (24) and (28), we have the equivalent circuit as follows:

$$\begin{bmatrix} \overline{V_{in}} - V_{th} \\ \overline{I_{in}} \end{bmatrix} = \begin{bmatrix} \frac{1}{2N} & 0 \\ 0 & 2N \end{bmatrix} \begin{bmatrix} 1 & R_{SC} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \overline{V_{out}} \\ -\overline{I_{out}} \end{bmatrix}. \tag{29}$$

Using (28) and (29), the equivalent circuit can be expressed by Fig. 13. When the output load is the resistive load R_L, the power efficiency η and the output voltage V_{out} are obtained as

$$\eta = \frac{R_L}{R_L + R_{SC}}\left\{\frac{2N\left(\overline{V_{in}} - V_{th}\right)}{2N\overline{V_{in}}}\right\} \tag{30}$$

and

$$\overline{V_{out}} = \frac{R_L}{R_L + R_{SC}}\left\{2N\left(\overline{V_{in}} - V_{th}\right)\right\}. \tag{31}$$

As (13), (18), (19), (28), (30), and (31) show, the power efficiency η and the output voltage V_{out} decrease according to the increase of the parameter N. However, the proposed voltage multiplier can alleviate the decrease of η and V_{out}, because the number of stages of the proposed multiplier is about a half of that of the conventional CWVM.

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