Bandpass Continuous-Time Delta-Sigma Modulator for Wireless Receiver IC

Huey Jen Lim, Simon Sheung Yan Ng and Minkyu Je

***Abstract*—Bandpass ADC is well known to be adopted in the narrowband receiver design in order to reduce the system complexity, increase integration and improve performance by digitizing the bandpass signal directly without prior conversion to baseband. A fully differential feedforward fourth-order continuous-time bandpass delta-sigma modulator is presented. The proposed single-bit modulator can receive 172.8kHz IF signals by using an oversampling clock frequency of 5.53MHz with an OSR of 128. Simulated result showing that dynamic range of 78dB within bandwidth of 21.6kHz is achieved and the current consumption is around 1.2mA at 1.5V power supply. The design had been implemented in 0.13µm 1P6M CMOS process with MIM capacitors.**

***Index Terms*—Analog-to-digital conversion, bandpass delta-sigma modulator, continuous-time**

I. Introduction

In the telecommunication system nowadays, designing of multi-standard receivers is the trend which can handle variety of modulation formats. Also, due to the limited resources in broadcast bandwidth, bandwidth-efficient modulation scheme is getting more and more popular and this has limited the bandwidth allocated for each communication channel. Thus, performing analog-to-digital conversion early in the receiver chain become imminent so as to move as much of the signal processing burden from the analog domain to the digital domain as possible. This results in robust radiofrequency receivers with high degree of programmability and adaptability to a number of standard specifications [1].

Conversion of narrowband analog signals thus is found in most telecommunications system nowadays including cellular telephony, radio and television. Bandpass delta-sigma modulators are very suitable for the implementation of ADCs in such systems. A bandpass ADC concentrates its conversion effort on the band of interest only, and can therefore be more efficient than an ADC which digitizes the entire band from dc to the IF. This characteristic offers advantage to the whole system in terms of lower power consumption to obtain a given dynamic range. Besides, by using the bandpass approach could keep the signal band away from dc and preserves the spectral separation between the signal of interest and various low-frequency noise sources and distortion components such as *1/f* noise and even order inter-modulation products.

Manuscript received June 1, 2012; revised August 27, 2012.

This work was supported in part by Cubic Micro, Inc. and Nagano Japan Radio Co., Ltd.

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II. System Architecture

Bandpass delta-sigma modulators are a particular class of delta-sigma modulators that place the zeroes of noise transfer function, NTF(f) in a given bandwidth around an intermediate frequency (IF) location, usually named as center frequency, f_c. The quantization noise is thus suppressed around the center frequency [2]. Continuous-time delta-sigma modulators could operate at higher clock frequencies and/or consume less power compare with its discrete-time counterpart. The block diagram of a continuous-time delta sigma modulator is as shown in Fig. 1. A loop-filter H(s) provides a noise-shaping function for the analog input signal before it is sampled and quantized by an ADC. The digital output signal is then converted back to analog signal by a DAC and feedback to the input for subtraction to form a close-loop operation. The continuous-time delta sigma modulation has intrinsic anti-alias filtering function. The input signal is sampled after being filtered through the continuous-time loop filter, significant suppression at aliasing frequencies can be obtained. Besides, since the sampler, f_s is placed inside the noise-shaping loop, any sampling error, together with quantization noise, is significantly suppressed by the high gain of the loop filter in the bandwidth of interest.

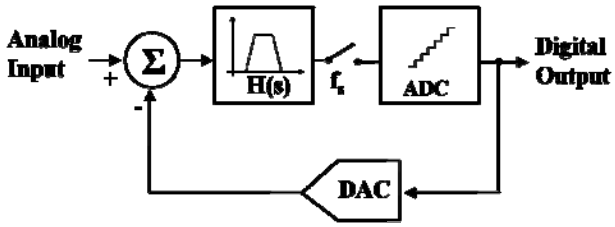


Fig. 1. Block diagram of continuous-time delta-sigma modulator.

Among the topologies used to implement the delta-sigma modulator, *chain of integrators with weighted feedforward summation* (CIFF) is a well known single-loop topology for low-voltage design due to its reduced output swing characteristics. Fig. 2 shows the architecture block diagram of the proposed fourth order bandpass continuous-time delta-sigma modulator. There are four integrators inside the topology to realize the fourth order system. Two local resonators are formed by the local feedback paths of *g1* and *g2*. These two local resonators place two zeroes around the center frequency, f_c and create the noise shaping function for the bandpass delta-sigma modulator. A half clock delayed of the output signal is fed back to the input of last integrator to compensate the excess loop delay issue which is inherent of a

DOI: 10.7763/IJIEE.2013.V3.252

continuous-time delta-sigma modulator [3].

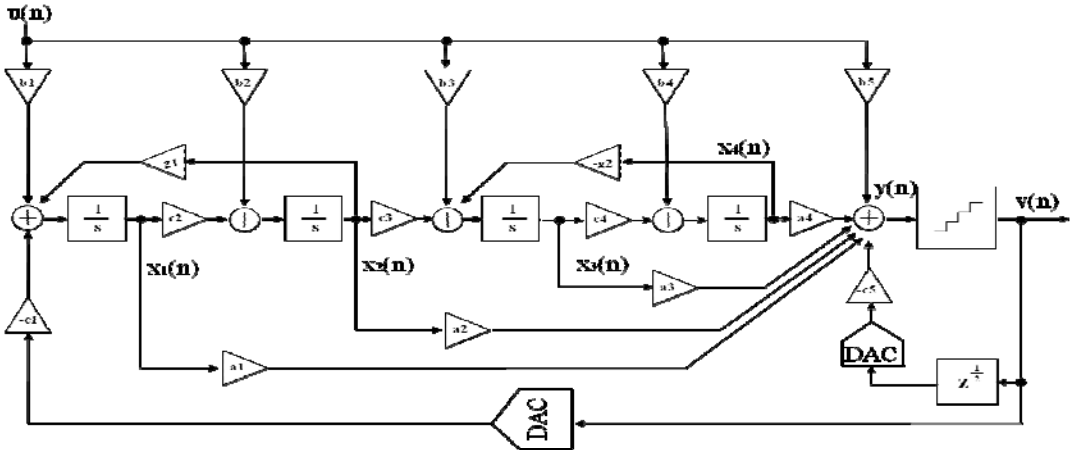


Fig. 2. Proposed system architecture for bandpass delta-sigma modulator

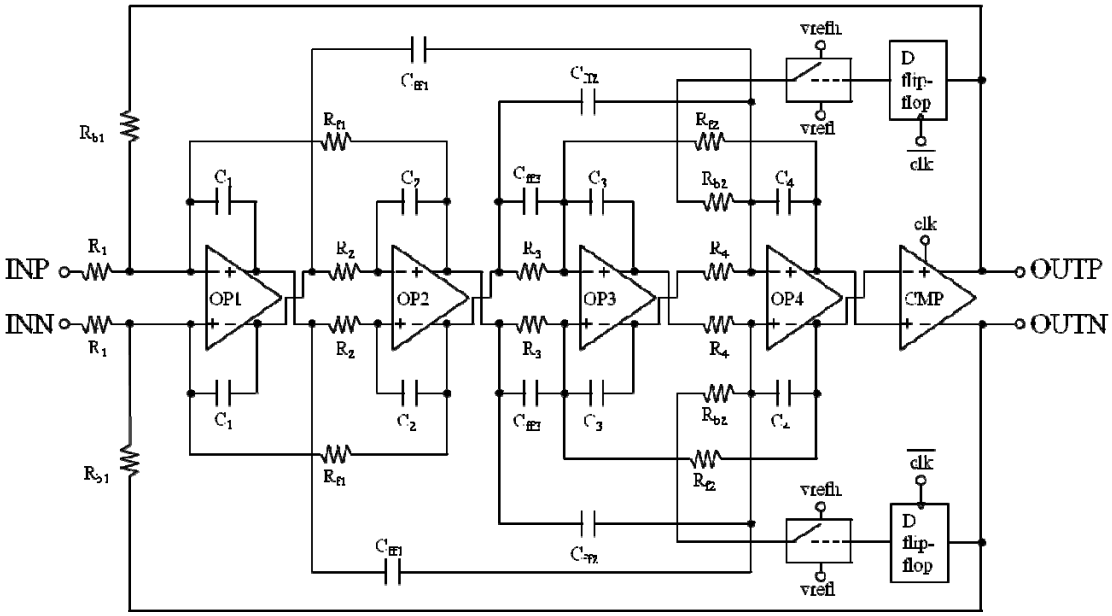


Fig. 3. Circuit implementation for the fully differential continuous-time bandpass delta-sigma modulator.

III. Circuit Implementation

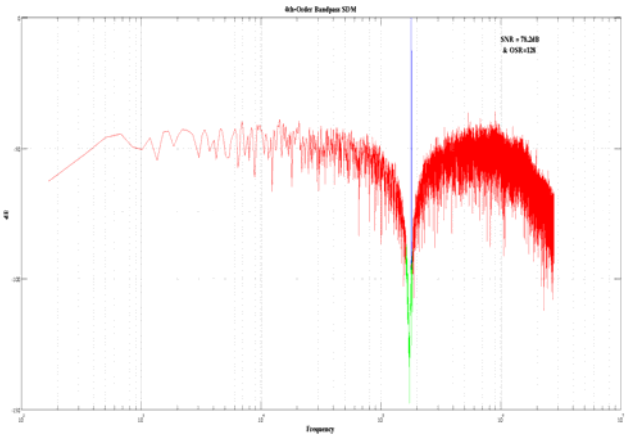
A circuit topology called *chain of integrators with weighted capacitive feedforward summation* (CICFF) is adopted to implement this design. The topology could eliminate the feedforward summation amplifier at the output of the filter and hence no additional power in the feedforward branches is consumed. All the feedforward summations are capacitive coupled to the last integrator and this design to achieve low voltage and low power consumption [4]. Among the practical continuous-time integrator structures, the active-RC integrator is chosen in the implementation because of its advantages of better linearity and large signal swing. All building blocks of the loop filter are implemented fully differentially. The feedforward coefficients *a1* to *a3* are realised as the ratios of the feedforward capacitances C_{ff1} ~ C_{ff3} to integration capacitance C_4. The feedforward coefficient *a4* is merged into the last integrator stage during the implementation. The feedforward capacitor C_{ff3} is moved to the previous integrator stage formed by OP3 to avoid the damping of the second local resonator [5]. The RC coefficients of *bi*, *ci* and *gi* are defined by the resistors R_i and capacitors C_i of the respective integrating stages. A detail circuit implementation of the modulator is shown in Fig. 3.

Four fully differential folded-cascode OTAs are used and configured as four integrators in the loop-filter design. The values of the integrating capacitors C_1 ~C_4 are carefully chosen to be bigger than the input and output capacitance of the OTA. Two local resonators that form by R_{f1} and R_{f2} added two zeros into the system near the centre frequency and suppress the noise in the specified bandwidth. A one-bit comparator is used to quantize the output of the last integrator and the digital output is directly feedback for subtraction. A D flip-flop with clk input is used to create half clock delayed of the digital output data. This signal is then passed to a multiplexer to choose the corresponding reference voltage verfh of vrefl and fed back to the last stage of the integrator, which form the excess loop delay compensation circuit.

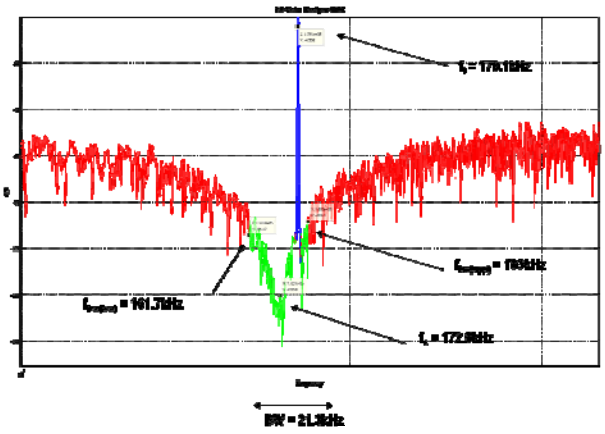
IV. Simulation Results

The simulated output power spectrum plot (32768 bins from 0 to sampling frequency) with 179.1kHz ($0.5V_{pk-pk}$) input signal for the delta-sigma modulator is depicted in Fig. 4(a). A zoom-in-view to the narrow bandwidth of interest around the center frequency, f_c of the output power spectrum

is shown in Fig. 4(b).



(a)



(b)

Fig. 4. (a) Simulated power spectrum density (32768-point FFT) plot.with 179.1kHz ($0.5V_{pk-pk}$) input signal, (b) A zoom-in-view.

TABLE I: PERFORMANCE SUMMARY

System Specifications Bandpass Continuous-time ΣΔ ADC	Value
Process Technology	0.13µm, 1P6M, CMOS
Center Frequency (IF frequency)	172.8kHz
Bandpass filter bandwidth	21.6kHz
Oversampling frequency	5.5296MHz
Oversampling Ratio	128
Order, Bit	4th, 1-bit
Dynamic Range	78dB
Power Consumption	1.2mA @ 1.5V
Silicon Area	830µm x 780µm

The spectrum shown in green is the bandwidth of interest while the input testing signal is shown in blue. The red portions are the unwanted signal and will be filtered off by the decimation filter. The desire noise shaping characteristic around the center frequency, f_c can be clearly seen from the figure. The noise level at the bandwidth of interest is suppressed and this has greatly improved the signal-to-noise ratio of the system. Dynamic range of 78dB could be achieved during the simulation.

V. CONCLUSION

In this paper, a fully differential feedforward fourth-order continuous-time bandpass delta-sigma modulator achieving a dynamic range of 78dB is presented. The narrowband modulator has been implemented in 0.13µm 1P6M CMOS process. The performance summary of the design is shown in Table I. The layout of the design is shown in Fig. 5 with the die area of 830 µm x 780µm.

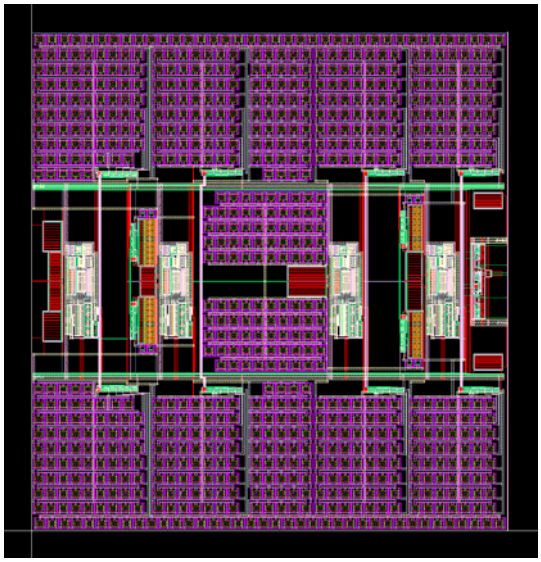


Fig. 5. Layout for the fully differential continuous-time bandpass delta-sigma modulator

ACKNOWLEDGMENT

The authors would like to thank Mr. Kumarasamy Raja Muthusamy for proof-reading this article and Ms. Josephine Jesalva Fernandez for layout support. The authors would also like to acknowledge Mr. Yoshihiko Tezuka from Nagano Japan Radio Co., Ltd., Japan and Mr. Atsushi Tamura from Cubic Micro KK, Japan for the technical discussions.

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