Circuit Implementations and Comparison between Different Multiplication Factors in Terahertz Frequency Generation in 90nm Process Using Linear Superposition

Avijit Saha, Shibani Ghosh, Md. Sakib Hasan, Ishraq Ahmed, and Avijit Das

***Abstract*—In this paper, the Linear Superposition technique for Terahertz frequency generation in CMOS circuits has been reviewed. The CMOS circuits are designed in 90nm process and oscillator parameters are designed to have a fundamental oscillation frequency of 91 GHz. Circuit designs for different values of multiplying factor N are demonstrated and their Pspice simulation results are presented and compared. In these simulations, oscillation of up to 910 GHz (for N=10) was observed.**

***Index Terms*—Terahertz frequency generation, linear superposition, terahertz CMOS circuits**

I. Introduction

With the continuous emergence of more and more new Terahertz (THz) signal applications, the necessity of evolution of novel design techniques to fill the so-called 'THz Gap' is on the rise. The attention has started to shift from traditional optically pumped lasers [1], backward-wave oscillators [2], direct-multiplied Sources [3], and quantum-cascade semiconductor lasers [4], towards digital CMOS technologies for generation of THz frequency signals. CMOS push-push oscillators have been implemented in [5]-[7] for generation of THz signals in the range of 0.1-0.5 THz. To overcome the limitation of push-push oscillators in maximum achievable oscillator frequency, a novel method of Linear Superposition has been demonstrated in [8]. In their paper [8], Huang *et al.* have devised a generalized algorithm of Linear Superposition (LS) of equally phase-shifted oscillations of same frequency to generate a frequency which is a multiple of the fundamental frequency of oscillation. The multiplying factor, denoted by N in [8], is equal to the number of superimposed phase shifted signals, and is a multiple of 2. Beginning their paper with a generalized algorithm for N=2k (k=1, 2, 3…), Huang *et al.* have demonstrated the circuit implementation for N=4, in 90 nm process, and have succeeded to generate 324 GHz frequency by this method.

This paper is directly motivated by [8], and looks into the LS method in a greater detail. In this paper, we have presented and described the circuit implementations for N=2, 4, 6, 8 and 10, and have been able to generate up to 910 GHz signal in simulation in 90nm process. The underlying mechanism and design techniques of the circuits are explained in detail, and the simulation results are presented and compared for different values of N.

The paper organization is as follows: Section II gives a review of the Linear Superposition method. Section III presents the analysis of the circuit for N=2 for explanation of the underlying principle of the circuit. Section IV describes the circuits for N=4, 6, 8 and 10 and their design techniques. The Simulation results are presented and compared in Section V. Finally, Section VI concludes the paper.

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II. Review of Linear Superimposition Technique

The basic principle of the LS technique has been described in [8], with mathematical formulation for the generalized case of N=2k. There is nothing new to present here regarding the theoretical explanation of the method. Still, a brief review is presented to give the reader an introduction to our work.

As the name suggests, the principle of the LS method lies in the linear superposition of different signals. In this case, the constituent signals are half-wave rectified oscillations of same fundamental frequency and are equally phase-shifted from one to the next. To achieve an equal phase-shift, for N number of constituent signals, the phase-shift between two adjacent signals should be $2\pi/N$. If N number of such signals are super imposed, they form a signal with frequency of N times the frequency of the fundamental oscillation. The phenomenon is explained in Fig. 1 for N=2 and 4.

In Fig. 1(a), two 180° phase-shifted signals are super imposed to generate a signal with frequency content of twice the frequency of the constituent signals. In Fig. 1 (b), for N=4, four half-wave rectified signals with 90° phase-shift between one to the next, are superimposed to generate a signal with frequency content of four times the fundamental frequency. Similar figures can be shown for N=6, 8, 10…etc. In general, the linear superimposed signal will contain the frequency $N*f_m$, if N number of signals, each with the fundamental frequency f_m, are used.

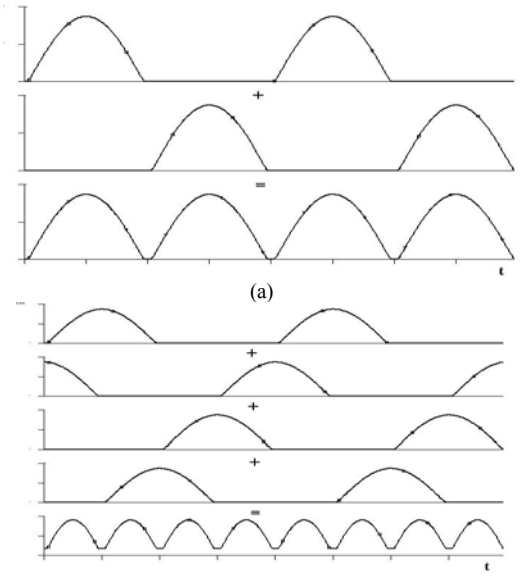
For a mathematical proof, one may refer to [8], which also shows the derivation of expression for fundamental to harmonic conversion ratio for the generalized case of N=2k, k=1, 2, 3 ... etc. The questions of how to generate N number of equally phase-shifted half-wave rectified oscillations of a particular frequency and how to superimpose them to

generate the multiplied frequency are answered in the following section.

III. Terahertz CMOS Circuit Analysis for N=2

The CMOS circuit implementation schematic for N=2 is given in Fig. 2. It should serve well to understand the principle of LS frequency generation. Circuit designs for higher values of N will be discussed in the next section.

The main part of the circuit in Fig. 2 is the LC tank oscillator. The cross-coupled connection between the MOSFETs M1 and M2, together with the L and C of the circuit helps to create and sustain an oscillation from the phase noise. The frequency of oscillation is determined by the size of the MOSFETs, and the values of L and C. We designed the circuit in 90nm process, with W/L=2.4μm/90nm for the MOSFETs. L and C were chosen to be 0.1nH and 0.02pF respectively. The load capacitances were given the value of 0.01pF. Supply voltages were V_{DD}=1V and V_{sup}=4V. For these values, the fundamental oscillation frequency fo was 91GHz. The generated output signals *Qp* and *Qm* (shown in Fig. 3(a)) of the oscillator at the drains of M1 and M2 have a phase shift of 180°, which is the required phase difference for N=2.



(a)

(b)

Fig. 1. Linear superimposition of equally phase-shifted signals for (a) N=2 and (b) N=4.

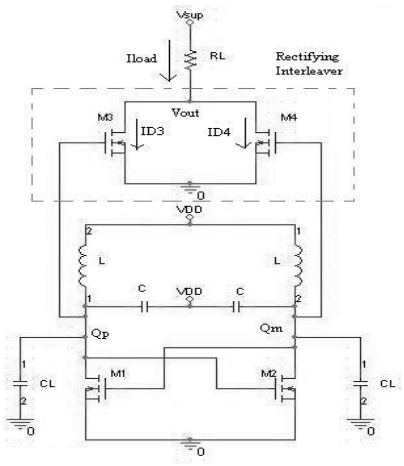


Fig. 2. CMOS circuit for LS N=2 implementation.

The rectification and linear superposition are both done by the rectifying interleaver circuit. As *Qp* and *Qm* are given at the gates of MOSFETs M3 and M4, they get turned on when the voltage at their gates exceed their threshold voltages. This causes the drain currents of the MOSFETs to be rectified for the voltage at their gates below threshold voltages. The drain currents I_{D3} and I_{D4} of the MOSFETs M3 and M4 are shown in Fig. 3(b). As both the currents are drawn from the supply voltage V_{sup}, they get linearly superimposed, because, to maintain Kirchhoff's Current Law, $I_{load}=I_{D3}+I_{D4}$. Finally, the current I_{load} causes a voltage drop across the load resistance R_L=50ohm with a similar waveform as the LS current. Hence voltage V_{out} is the LS waveform which contains the frequency f_{out}=2*91 GHz=182 GHz, as shown in Fig 3(c).

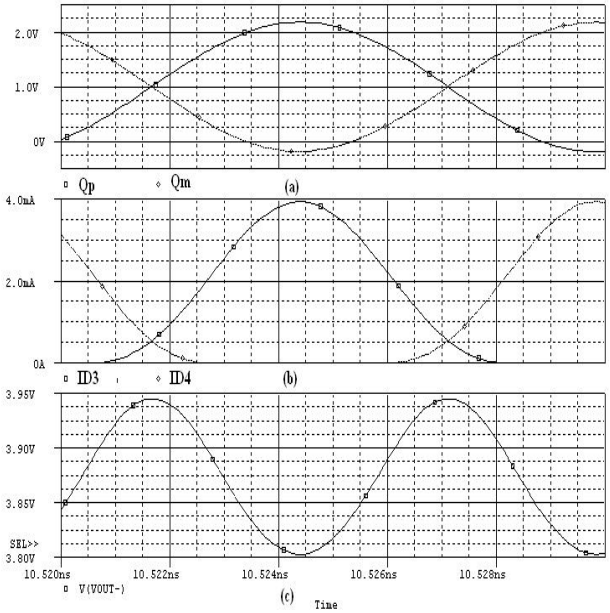


Fig. 3. Simulation results for LS N=2: (a) qm and qp, (b) ID3 and ID4, (c) vout.

IV. CMOS Circuit Designs For Higher Values of N

The basic principle being the same as explained in the previous section for N=2, the circuit designs for higher values of N only have the challenge of appropriate cross-coupling of multiple LC tank oscillators to generate the equally phase-shifted oscillations. The circuit implementation schematics for N=4, 6, 8 and 10 are shown in Fig 5.

For N=4 (Fig. 5(a)), two LC tank oscillators are cross-coupled by MOSFETs M5, M6, M7 and M8. The gates of M5 and M6 are connected to drains of M7 and M8 respectively, but the gates of M7 and M8 are reversely connected to the drains of M6 and M5 respectively.

For N=6 (Fig. 5(b)), three LC tank oscillators are cross coupled. In this case, for two pairs of adjacent oscillators, the coupling between MOSFETs is straightforward, but the third pair is coupled in a reverse coupling connection between MOSFETs (gate of M11 to drain of M8, gate of M12 to drain of M7).

For N=8 (Fig. 5(c)), four LC tank oscillators are cross-coupled. This time, three adjacent pairs are coupled in straightforward manner, only one pair is coupled with reverse connection.

For N=10 (Fig. 5(d)), three pairs of five LC tank oscillators

are coupled in a straightforward manner, the other two pairs are coupled with a reverse connection.The connections described are necessary for the generation of equally phase-shifted oscillations and hence are mandatory for the circuit designs. The problem with finding a general pattern for number of straightforward and reverse coupling connections for a particular N lies in the fact that for higher values of N, the power in the harmonic is too low to be observed even in simulation.

V. Simulation Results

All the circuits demonstrated so far were simulated in Pspice. The phase-shifted oscillations and final output waveforms for N=4, 6, 8 and 10 are shown in Fig. 6(a), (b), (c) and (d) respectively (Simulation results for N=2 has already been shown in Section III). The generated frequencies were 364 GHz, 546 GHz, 728 GHz and 910 GHz for N=4, 6, 8 and 10 respectively.

The frequency values, output voltage peak to peak values, average power consumption of the circuits and number of MOSFETs required (an approximate measure for required chip area) for different values of N are tabulated in Table I for comparison.

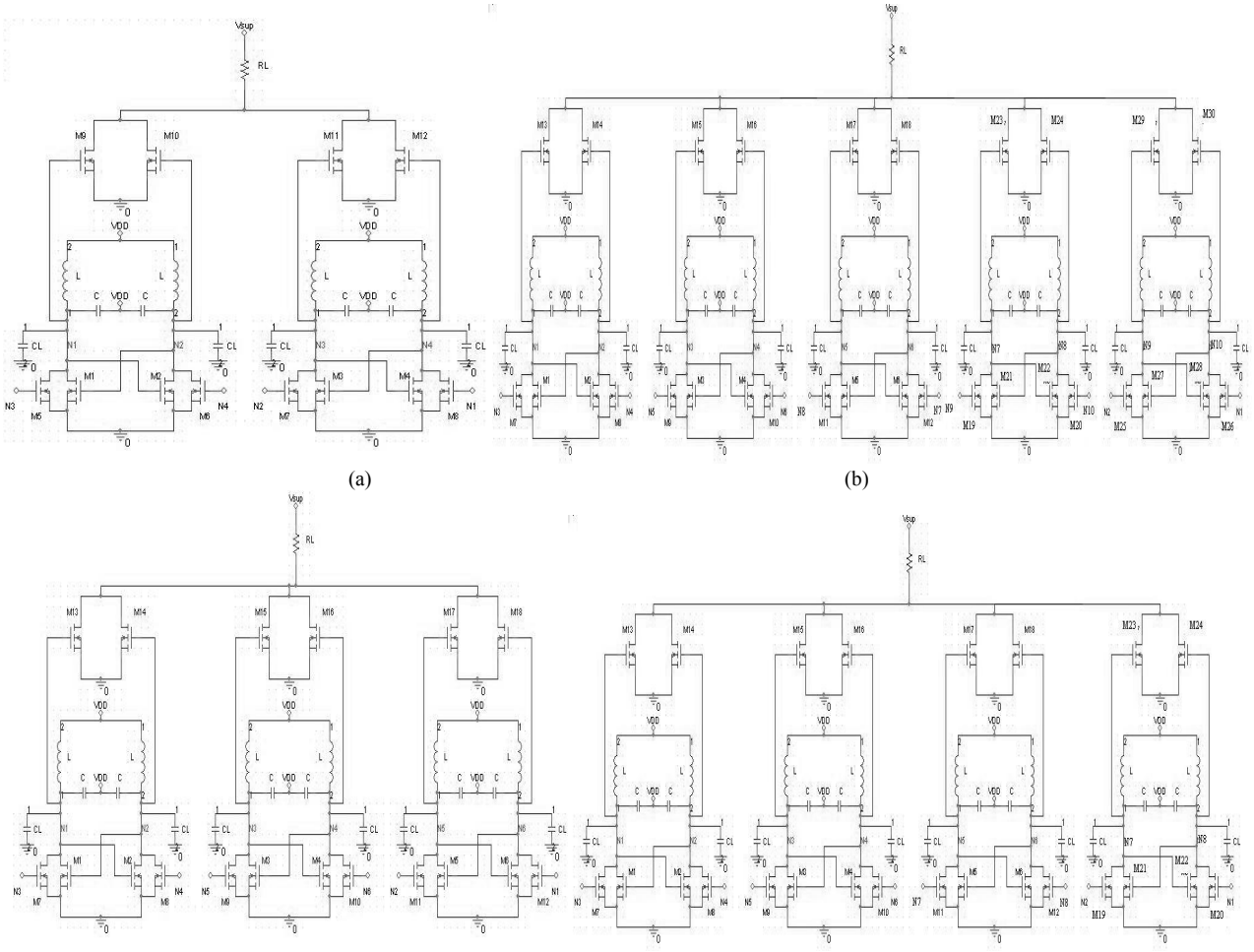
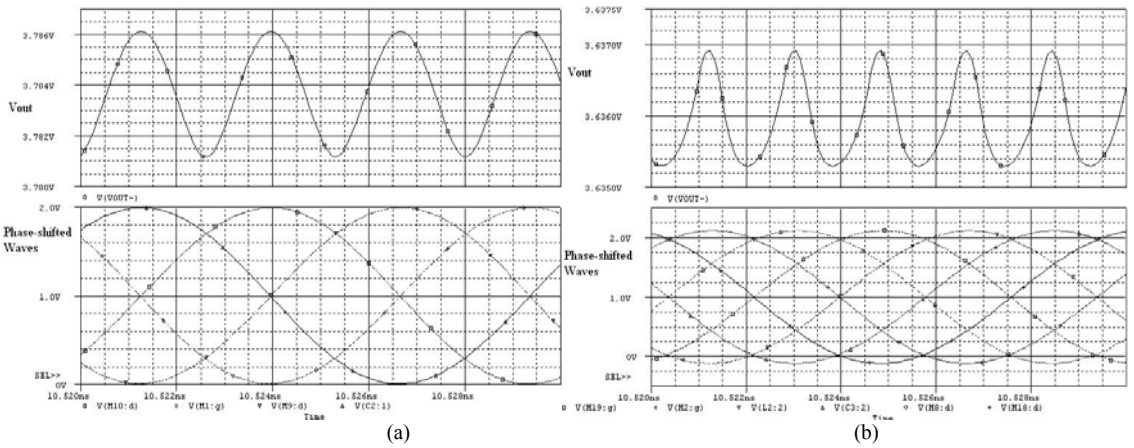
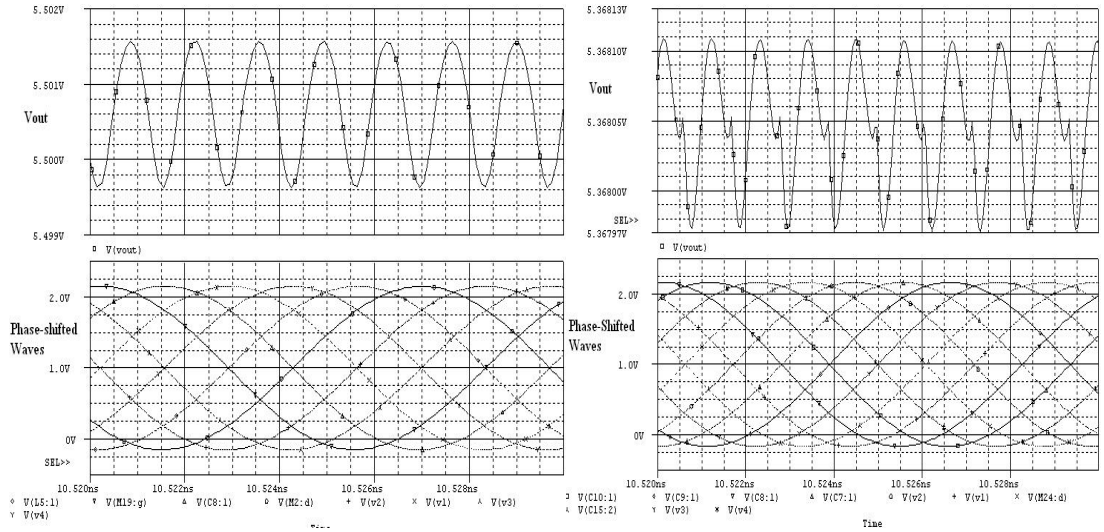


Fig. 4. CMOS circuit implementations for (a) N=4 , (b) N=6, (c) N=8, (d) N=10.





(c) (d)

Fig. 5. Phase-shifted waveforms and output voltage waveform for (a) N=4, (b) N=6, (c) N=8 and (d) N=10.

As we can see in Table I, with increasing N, area and power consumption increases, but the yield is decreased. This was also predicted from theoretical calculations in [8].

TABLE I: COMPARISON BETWEEN DIFFERENT VALUES OF N

Parameter	N=2	N=4	N=6	N=8	N=10
Generated Frequency	182 GHz	364 GHz	546 GHz	728 GHz	910 GHz
Peak-to-peak Output Voltage	142.5 mV	5 mV	1.6 mV	1.2 mV	0.14 mV
Power Consumption	10.675 mW	18.275 mW	30.11 mW	60.947 mW	76.954 mW
Number of MOSFETs	4	12	18	24	30

VI. CONCLUSION

The LS method of Terahertz signal generation using CMOS circuits has been comprehensively reviewed. The circuit operation has been explained and circuit design considerations have been discussed for multiplying factor N=2, 4, 6, 8 and 10. Pspice simulation results for these circuits have been presented and compared. The maximum frequency of 910 GHz for N=10 was generated in simulation. This paper should assist [8] to have a better understanding of the Linear Superposition method in Terahertz signal generation and its possibilities to fill the 'THz Gap'.

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