Low Power Voltage Controlled Ring Oscillator Design with Substrate Biasing

Manoj Kumar, Sandeep K. Arya, and Sujata Pandey

Abstract—**In the present work, improved designs for voltage controlled ring oscillators (VCO) with reverse body bias technique have been presented. In the proposed designs, output frequencies of VCOs have been controlled by varying the reverse bias voltage with improvement in power consumption. First VCO design with five inverter based delay cell shows frequency variation [1.3733-1.1218] GHz with varying NMOS substrate bias voltage from 0.0V to -1.5V. Second design with varying PMOS substrate bias from [1.8-3.3] V shows frequency variation of [1.3733-1.0009] GHz. Further, third design with joint substrate biasing of NMOS and PMOS transistors shows frequency variations [1.3251-0.81837] GHz. Power consumption has been reduced with reverse body bias in three proposed circuits Simulations have been performed by using SPICE based on TSMC 0.18µm CMOS technology. Power consumption of VCOs circuit has been compared with earlier reported circuits and proposed circuit's shows better performance.**

Index Terms—**CMOS, low power, substrate bias and voltage controlled oscillator.**

I. Introduction

The Voltage controlled oscillators (VCO) are the critical and necessary component in data communication systems and have wide applications in modulation, demodulation and clock recovery circuits etc. Two widely used VCOs types are CMOS ring and LC tank based circuits. The on chip combination of inductor and capacitor consumes large layout area in LC tank based oscillators [1]-[3]. CMOS based ring inverter oscillators have advantages over other oscillators design due to ease of controlling the tuning range and no requirement for on chip inductors [4], [5]. CMOS based ring oscillators also have a wide tuning range and are easier to integrate in CMOS process. Due to flexibility for on chip integration, CMOS based ring oscillator has become essential building blocks in various very large scale integration (VLSI) systems with wide applications in battery operated mobile devices.

A ring oscillator is composed of delay stages along with feedback from output to input stage. Different types of ring VCOs have been reported using different types of delay cells including multiple-feedback loops, single ended delay cells and dual-delay paths [6]-[10]. A single ended inverter based ring VCO block diagram is shown in fig.1

Manuscript received January 8, 2012; revised February 29, 2012.

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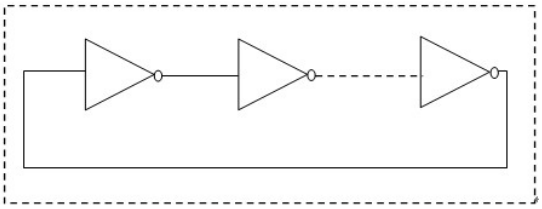


Fig. 1. Block diagram of single ended VCO.

For oscillation occurrence, the ring must provide a phase shift of 2π and should have unity voltage gain. Each delay stage should provide phase shift of π/N, where N is number of delay stages. The remaining π phase shift is provided by dc inversion. Single ended oscillator requires odd number of stages for dc inversion. Frequency of oscillation for N stage delay ring VCO is given by $f_o = \frac{1}{2Nt_d}$, where N is the number of delay stages and t_d is delay of each stage [11], [12]. VCO is the indispensable components in PLL (Phase locked loop) and also responsible for most of the power consumption of PLL. Some draw backs of ring based oscillators includes large power consumption, phase noise and the limit of highest achievable frequency. In modern VCOs power consumption and frequency tuning are key performance metrics [10], [12]-[17]. Growing demand of portable devices like cellular phones, notebooks, personal communication devices have aggressively enhanced attention for the low power consumption. Power consumption in VLSI circuit includes dynamic, static power and leakage power consumption. Dynamic power consumption results from switching of load capacitance between two different voltages and dependent on frequency of operation. Whereas static power is contributed by direct path short circuits currents between supply (VDD) and ground (VSS) and dependent on leakage currents [18], [19]. Leakage power results from leakage currents that arise from substrate injection and sub-thresholds currents. The scaling trends of MOSFETs lead to the developments towards nano-scale which further increases the leakage currents. Static power component of power dissipation is also playing a very important role in the total power consumption beside dynamic power. Controlling the bulk terminal of CMOS device offers improved performance in term of power dissipation [20]. To reduce the standby leakage in CMOS circuits, a reverse body biasing is generally used. Body biasing techniques make use of body terminal as another control mechanism to dynamically tune the threshold voltage [21].

In present work three modified VCO circuits have been presented with reduced the power consumption and output frequency have been controlled by reverse bias voltage. The paper is organized as follows: In section II three different five stage inverter based ring VCOs using reverse bulk

biasing have been presented. In section III results for the three proposed VCOs have been obtained and comparisons with earlier reported structures have been presented. Finally, in Section IV conclusions have been drawn.

II. System Description

Bulk terminal of PMOS and NMOS have been used for controlling the output frequency and reduction in power consumption in VCO structure. By application of reverse body bias, the V_{th} is increased as given in equation (1), which subsequently reduces the sub threshold leakage currents [19], [21]. Threshold voltage (V_{th}) is related by the square root of the bias voltage implying that a considerable voltage level would be needed to raise the V_{th}. By controlling bulk voltage (V_{sb}) leakage current are minimized and hence power consumption is reduced.

$$V_t = V_{t0} + \gamma\left(\sqrt{2\phi_f + V_{sb}} - \sqrt{2\phi_f}\right) \quad (1)$$

where V_{t0} is threshold voltage for $V_{sb} = 0V$; ϕ_f is Fermi potential and γ is substrate bias coefficient.

CMOS inverter has been utilized as delay element in the proposed circuits. Each inverter stage is made up of NMOS and PMOS pair and body terminal of transistors are not connected to source. A small capacitance of 0.01pf at output of each delay cell has been included. The circuits have been designed in 0.18µm CMOS technology with supply voltage of 1.8V. The gate lengths of NMOS and PMOS have been taken as 0.18µm whereas widths of PMOS and NMOS have been taken as 1.25µm and 0.50µm respectively. Three different circuits have been presented in which output frequency is controlled by reverse body biasing with reduced power consumption.

In first proposed circuit, a five stage ring VCO with varying bulk control voltage (V_{cbn}) has been shown in Fig. 2. Body terminal of all PMOS transistors have been connected to V_{dd} whereas the reverse bias voltage (V_{cbn}) of all NMOS transistors has been varied from [0.0 to -1.5] V. Supply voltage also have been varied from 1.8 to 1.0V to obtain the effects of revere bias with different supply voltages.

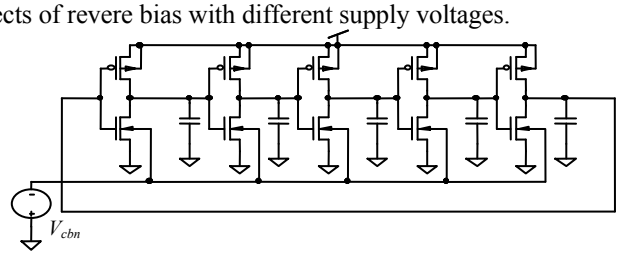


Fig. 2. Five stage ring VCO with NMOS reverse substrate bias.

Fig. 3 shows a modified five stage ring VCO with NMOS substrate terminal biased to ground whereas all PMOS body terminal are connected to varying bias control voltage (V_{cbp}). In this circuit bias voltage of PMOS transistor (V_{cbp}) are varied from [1.9-3.3] V keeping all NMOS body terminals at ground. Output frequency and power consumption are obtained for various values of PMOS substrate bias (V_{cbp}). Supply voltage also has been varied from 1.8 V to 1.0 V and output frequency and power consumption have been obtained with different voltages.

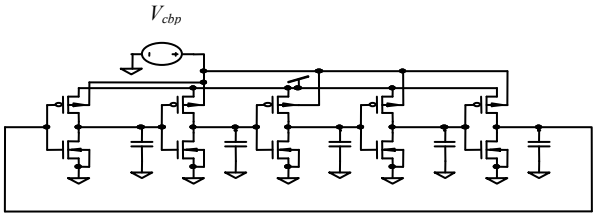


Fig. 3. Five stage ring VCO with PMOS reverse substrate bias

In third proposed circuit NMOS substrate bias (V_{cbn}) and PMOS substrate bias (V_{cbp}) have been varied simultaneously as shown in Fig. 4. All PMOS transistor substrate terminal have been biased to V_{cbp} which has been varied from 1.9 to 3.3V. All NMOS body terminal have been connected to V_{cbn} which is varied from 0.1 to 1.5V. Supply voltage also has been varied from 1.8 V to 1.0V. Output frequency have been controlled by combination of NMOS, PMOS reverse biasing and supply voltage variation.

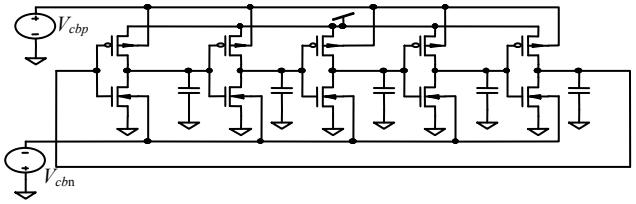
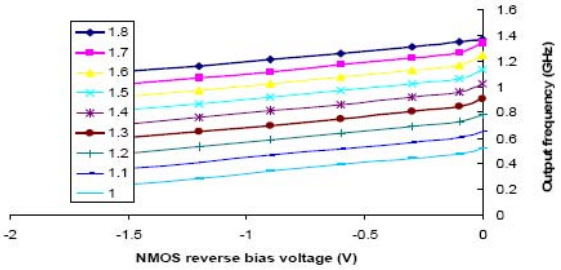


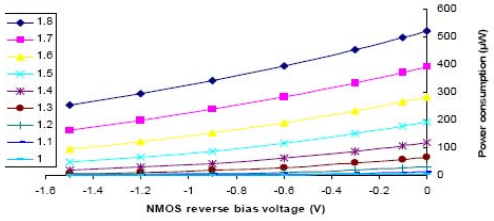
Fig. 4. Five stage ring VCO with joint NMOS & PMOS reverse substrate bias.

III. Results and Discussions

Simulations have been performed using SPICE based on TSMC 0.18µm technology with supply voltage variations from [1.8-1.0] V. Reverse bulk voltage has been used to control the output frequency and power consumption at different supply voltages. With a constant supply voltage a full output swing is obtained without compromise in output level which is the advantages of proposed designs. Output frequency has been controlled with reverse bias voltage without changing the supply voltage. Fig. 5(a) shows the result of output frequency variation with varying NMOS substrate bias at different supply voltages. It has been observed from the results that output frequency varies with change in reverse bias at different supply voltages. Fig. 5(b) shows power consumption variation with reverse bias at different supply voltages. At supply voltage of 1.8 V, output frequency varies from [1.3733-1.1218] GHz with change in reverse bulk control voltage from [0.0 to -1.5] V. Power consumption also has been reduced from 520.5468µW to 252.9188µW with varying reverse bias [0.0 to -1.5] V. At lower side with 1.0 V supply voltage, frequency varies from [0.51497 to 0.23422] GHz and power varies from [3.7650 to 0.176194] μW with reverse bias variation. Results also show that power saving is improved with application of reverse bias at different supply voltage as compared to circuit with null reverse bias. Fig. 6 shows output waveforms for five stages ring VCO with NMOS reverse bias of -0.6 V at supply voltage of 1.8 V.



(a)



(b)

Fig. 5.(a) Output frequency (b) Power consumption variation with NMOS substrate bias at different supply voltages.

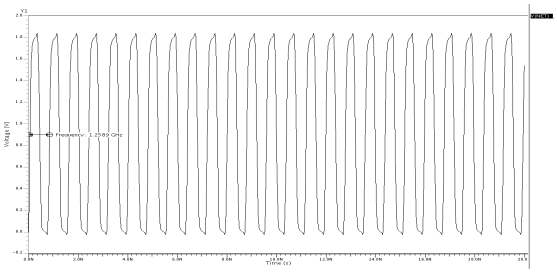
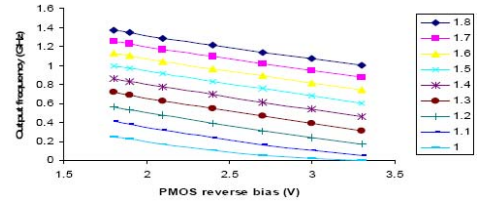
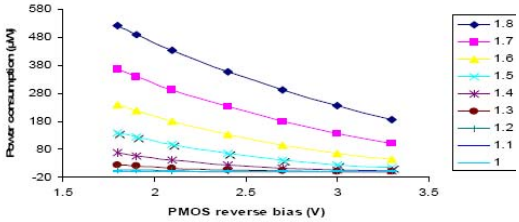


Fig. 6.Output waveform at -0.6V NMOS substrate bias with 1.8V supply.

Fig. 7(a) & 7(b) shows the results for proposed VCO with varying PMOS reverse bias [1.9-3.3] V with all NMOS body terminal at ground. At supply voltage of 1.8 V, output frequency varies from [1.3733 to 1.0009] GHz with the varying PMOS reverse bias from [1.8-3.3] V. Power consumption has been reduced from [520.5468 to 186.6156] µW with variation in PMOS substrate bias [1.8-3.3] V. It has been observed from fig.7(b) that power consumption is reduced with PMOS substrate bias at different supply voltages. Fig. 8 shows the output waveform results for 2.4V PMOS reverse substrate bias.



(a)



(b)

Fig. 7.(a) Output frequency (b) Power consumption variation with PMOS substrate bias at different supply voltages.

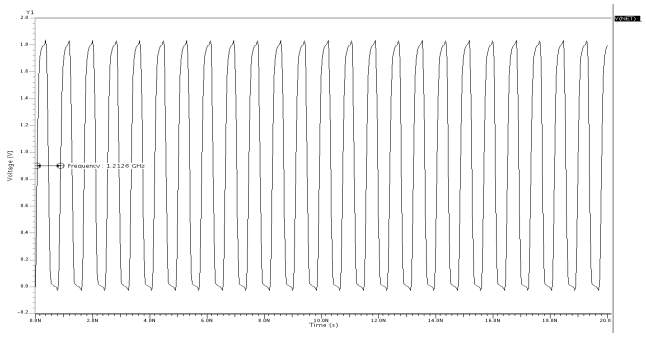
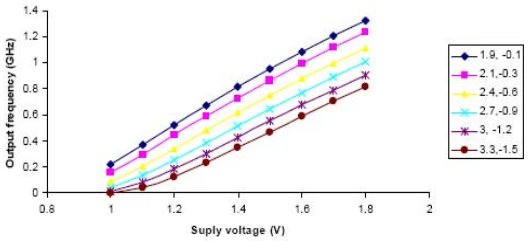
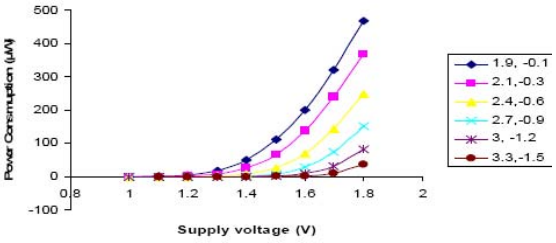


Fig. 8. Output waveform at 2.4V PMOS substrate bias with 1.8V supply.

Fig. 9 (a) & 9(b) shows the simulation results for third proposed ring VCO with joint biasing of NMOS & PMOS transistors at different supply voltages. Output frequency and power consumption shows variation [1.3251 to 0.81837] GHz & [466.9918 to 37.2683] µW with simultaneous change of NMOS & PMOS reverse bias voltage. Tuning range has considerably increased with joint substrate biasing of NMOS & PMOS transistor as compared to previous circuits. Power consumption also shows improvement with joint substrate biasing. Fig. 10 shows the output waveform results for 2.4V PMOS & -0.6V NMOS reverse substrate bias voltage.



(a)



(b)

Fig. 9. (a) Output frequency (b) Power consumption variation with joint reverse biasing of PMOS & NMOS

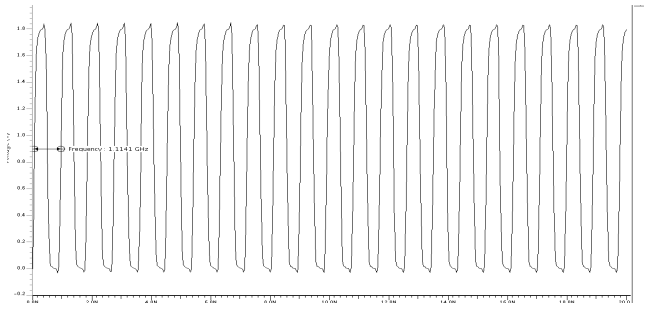


Fig. 10. Output waveform with -0.6 V NMOS & 2.4V PMOS substrate bias.

A comparison with earlier reported circuits in terms of power consumption and output frequency range is given in Table I. Proposed VCO circuits' with reverse body bias shows better performance than earlier reported circuits.

TABLE I : COMPARISON OF VCO PERFORMANCE

VCO designs	Operating frequency (GHz)	VDD (V)	Technology (μm)	Power consumption (mW)
[4]	0.39-1.41	1.8	0.18	12.5
[3]	2.17-2.73	0.9	0.18	2.7
[17]	0.65-1.6	1.8	0.18	39
[13]	0.12-1.3	0.5	0.18	0.085
[16]	1.57-3.57	1.8	0.090	16.8
Present work (NMOS biasing)	1.1218-1.3733	1.8	0.18	0.520
Present work (PMOS biasing)	1.009-1.3733	1.8	0.18	0.520
Present work (Joint biasing)	0.81837-1.3251	1.8	0.18	0.467

IV. CONCLUSIONS

In reported work three improved designs for five stage CMOS inverter based VCO have been presented. By controlling of reverse body bias power consumption has been reduced and output frequency has been controlled with the advantage of full swing output signal. Controlling the bulk terminal provide alternative method to control the output frequency with reduced power consumption. For first proposed VCO frequency range of [1.3733 to1.218] GHz has been obtained with varying NMOS revere biasing at supply voltage of 1.8V. In second proposed circuit output frequency shows variation [1.3733 to1.0009] GHz with varying PMOS substrate bias at 1.8V supply voltage. Output frequency rage [1.3251 to 0.81837] GHz has been obtained with joint biasing of NMOS & PMOS transistors with 1.8 V supply voltage. Power saving can be achieved by applying reverse biasing with constant supply voltage for those applications in which limited frequency variation is desired.

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